MRAM for ARINC 664 (AFDX), similar deterministic Automotive and Industrial Systems

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How PERSYST™ MRAM supports deterministic data handling, packet buffering and persistent data capture across avionics, automotive and industrial Ethernet systems.

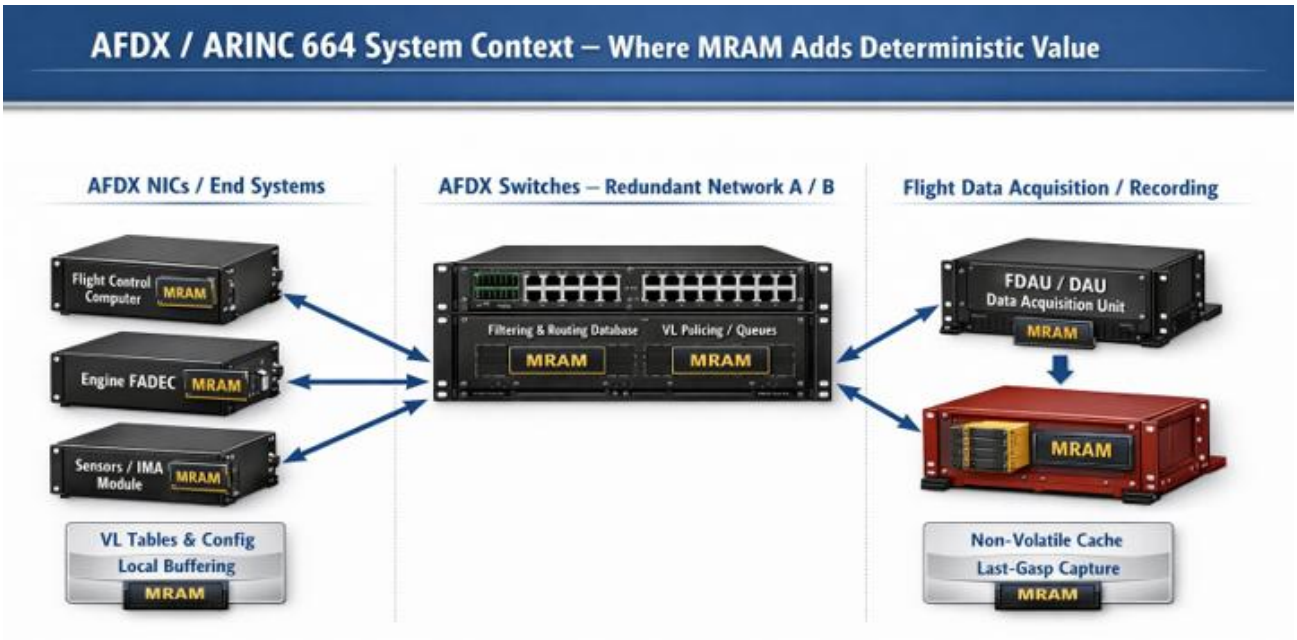


Figure 1: Potential MRAM insertion points in an ARINC 664/AFDX network.

In the transition from traditional bus-based avionics (MIL-STD-1553) to switched Ethernet networks (ARINC 664/AFDX), the volume and velocity of data have increased by orders of magnitude. For the Airbus A380, Boeing 787 and modern military aircraft, the challenge is no longer just moving data but ensuring determinism and persistence in the event of power loss or radiation events.

Traditional memory architecture of coupling SRAM for speed with Flash for non-volatility creates a bottleneck in high-bandwidth applications. Deterministic environments in similar vertical markets, such as automotive and industrial, also demand high reliability and longevity. Everspin *PERSYST* MRAM offers a "Universal Memory" solution that consolidates these roles into a single, high-reliability solution for the required packet buffering, routing tables and high-resolution data logging.

While ARINC 664 (AFDX) is not yet the dominant standard in low Earth orbit (LEO) like it is in commercial aviation, it is actively being transitioned into the space domain as part of a push

toward Integrated Modular Avionics (IMA) for Space. Research projects like MISSION have already confirmed the feasibility of using AFDX for spacecraft onboard data networks, demonstrating its ability to handle high-traffic, real-time communications in space environments.

Where MRAM Fits in ARINC 664/AFDX Networks

In an ARINC 664 network, three primary electronic components can significantly benefit from the use of MRAM:

AFDX Network Interface Controllers (NICs) / End Systems

These are the "smart" interfaces on every avionics subsystem (flight control, engines, cabin systems) that bridge the local CPU to the AFDX network.

- ✓ Virtual Link (VL) Descriptor Storage.
- ✓ AFDX relies on Virtual Links to manage deterministic bandwidth, requiring constant access to the descriptor tables that define them. By utilizing MRAM with an Expanded Serial Peripheral Interface (xSPI) supporting clock rates of up to 200 MHz in Single Transfer Rate (STR) or Double Transfer Rate (DTR) mode, with DTR throughput of up to **400 MBytes/s**, these tables are updated in real-time. This high-speed throughput eliminates the "busy" wait states and latency penalties inherent to Flash, ensuring seamless link management.

AFDX Switches

The "brain" of the network that routes packets between End Systems.

- ✓ Packet Buffering and Filtering Databases.
- ✓ Switches must buffer incoming frames before forwarding. In high-traffic scenarios, standard Flash would wear out in weeks due to the sheer volume of write cycles. MRAM's infinite write **endurance** (10^{14} cycles on each 32-Byte endurance unit) allows it to act as a high-speed buffer that never wears out. Additionally, its SEU (single-event upset) **immunity** ensures that routing tables are not corrupted by cosmic radiation, preventing "lost" or misdirected flight-critical packets.

Flight Data Acquisition Units (FDAU)

Aggregating mission-critical sensor data across the network for "black box" recording.

- ✓ Non-Volatile Data Cache.
- ✓ In the event of a catastrophic power failure, the last several milliseconds of data are often lost because they are sitting in volatile SRAM waiting to be written to slow Flash. MRAM is **inherently non-volatile**; as soon as a 32-Byte endurance unit is written, in as little as 145 nanoseconds, it is safe. This ensures 100% data capture up to the moment of failure without the need for large, unreliable "super-capacitors."

Strategic Advantages of Everspin *PERSYST* in ARINC 664

- ✓ **Radiation Resilience (LEO and High-Altitude):** Unlike charge-based memories (SRAM/Flash) that suffer from bit-flips in space or at high altitudes, MRAM stores data magnetically and is immune to **single-event latch-up (SEL)**, making it well-suited for LEO satellite constellations using AFDX-like protocols. Refer to independent test reports for additional details.
- ✓ **SWaP-C (Size, Weight, Power, and Cost) Optimization:** By replacing two chips (SRAM + Flash) with one MRAM device, designers reduce PCB footprint and weight, lower the power budget (no wear leveling or page erase required) and cut cost by simplifying the bill of materials (BOM).

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- ✓ **Deterministic Timing:** ARINC 664 is all about bounded latency. MRAM's lack of "garbage collection, block erase and wear-leveling" (required by Flash) means the memory response time is identical every single time, supporting the strict determinism required by FAA/EASA certification as well as various automotive and industrial standards.
- ✓ **Long-Term Availability:** Everspin's long-term supply gives designers the confidence to design MRAM into their military, aerospace, automotive or industrial solutions without worrying about obsolescence or requalification from constant product changes. Everspin continues to provide products introduced 20 years ago.

ARINC 664/AFDX is a strong aerospace reference point, but the same memory bottlenecks also appear in automotive and industrial deterministic Ethernet systems. Frequent table updates, high-write buffering and assured data capture through power disturbance all create similar demands, making the same MRAM advantages directly relevant beyond avionics.

Beyond ARINC 664: Other Deterministic Systems

Automotive: TSN (Time-Sensitive Networking) and ISO 26262

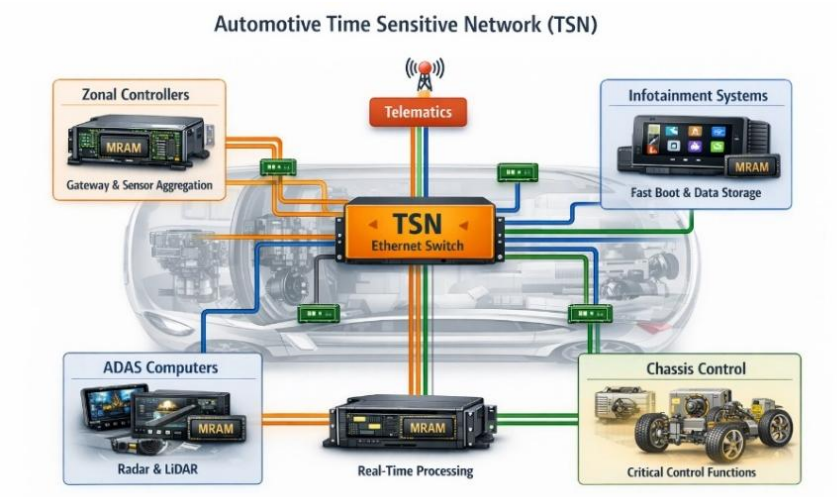


Figure 2: Automotive TSN network showing potential MRAM use across zonal, ADAS, infotainment and chassis systems.

Modern vehicles are moving toward Automotive Ethernet (TSN) to handle ADAS (Advanced Driver Assistance Systems) and autonomous driving data.

- ✓ Used in Zonal Controllers and ADAS Computers.
- ✓ Everspin's *PERSYST* High Reliability **AEC-Q100 Grade 1** qualification (-40°C to +125°C) is mandatory. MRAM provides a reliable "black box" for crash-data that cannot be corrupted by electrical noise or power loss. Furthermore, OTA updates for engine or safety maps are simple and more than 2,000 times faster, by eliminating the need for Flash File System software overhead of bad block mapping, block erasing and wear-leveling, MRAM allows for safe, high-speed updates even during brief vehicle "wake" cycles.

Industrial: PROFINET IRT and EtherCAT®

High-end factory automation uses **PROFINET IRT (Isochronous Real-Time)**, which, like AFDX, uses switched Ethernet for sub-millisecond control of robotics.

- ✓ PLC (Programmable Logic Controller) State Storage.
- ✓ Industrial environments are "electrically noisy." MRAM's magnetic storage is highly resistant to the electromagnetic interference (EMI) found near high-voltage motors. It also allows for zero-maintenance operation; because MRAM doesn't need a backup battery to save the PLC state during a power outage, factory owners save thousands on long-term maintenance costs and avoid downtime from dead batteries.

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Across ARINC 664, Automotive TSN, and Industrial EtherCAT®/PROFINET IRT designs, the common requirement is deterministic, high-endurance non-volatile memory matched to system bandwidth, temperature range and qualification needs. Everspin's *PERSYST* product portfolio addresses these design points with Quad and Octal xSPI interface options, allowing designers to select the right balance of reliability, interface speed, density and environmental grade for each implementation.

PERSYST xSPI Interface Product Portfolio

Everspin's xSPI Spin-Transfer Torque MRAM (STT-MRAM) portfolio addresses two distinct deterministic system design priorities. The Quad xSPI family is the best fit for applications that prioritize high reliability, broad qualification coverage and automotive-grade operation, supporting clock rates up to 133 MHz STR (up to 66.5 MB/s) and 90 MHz DTR (up to 90 MB/s), with AEC-Q100 Grade 1 options up to +125°C.

xSPI STT-MRAM Quad I/O (up to 90 MB/s)				
Product Family	**Density**	**Grade**	**Temperature**	**Packages**
EM004LXQ	4Mb	Commercial Industrial, Industrial Low Power "SC" Extended	0 to +70C -40 to +85C -40 to +105C	8-DFN (5x6 mm) 24-BGA (6x8 mm)
EM008LXQ	8Mb			
EM016LXQ	16Mb			
EM032LXQ	32Mb	Commercial Industrial, Industrial Low Power "SC" Extended AEC-Q100 Grade 1	0 to +70C -40 to +85C -40 to +105C -40 to +125C	8-DFN (6x8 mm) 24-BGA (6x8mm)
EM064LXQ	64Mb			
EM128LXQ	128Mb	Commercial Industrial Extended AEC-Q100 Grade 1	0 to +70C -40 to +85C -40 to +105C -40 to +125C	8-DFN (6x8 mm) 24-BGA (6x8 mm)
EM256LXQ	256Mb	Commercial Industrial Extended AEC-Q100 Grade 1	0 to +70C -40 to +85C -40 to +105C -40 to +125C	24-BGA (6x8 mm)

The Octal xSPI family targets designs that need maximum interface bandwidth for fast configuration updates and high-rate data logging, delivering up to 400 MB/s at 200 MHz DTR. Available in Commercial, Industrial and Extended temperature grades (up to +105°C), it is well suited to applications where interface speed, rather than AEC-Q100 or High Reliability qualification, is the primary selection driver.

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xSPI STT-MRAM Octal I/O (up to 400 MB/s)				
Product Family	**Density**	**Grade**	**Temperature**	**Package**
EM004LXO	4 Mb	Commercial Industrial Extended	0 to+70C -40 to +85C -40 to +105C	24-BGA (6x8 mm)
EM008LXO	8 Mb			
EM016LXO	16 Mb			
EM032LXO	32 Mb			
EM064LXO	64 Mb			
EM128LXO	128 Mb			
EM256LXO	256 Mb			

Together, these families allow designers to align interface speed, environmental requirements and qualification needs to target ARINC 664, Automotive TSN, or Industrial EtherCAT®/PROFINET IRT implementation.

Takeaways: MRAM for Deterministic Systems

- **Deterministic timing:** consistent read/write behavior with no erase-induced latency spikes.
- **Practically unlimited endurance** supports continuous buffering and high-rate logging without wear-out.
- **True non-volatility:** data is safe immediately, enabling robust "last gasp" capture without oversized energy storage.
- **High reliability for harsh environments:** resilient against radiation and EMI compared with charge-based memories.
- **Architecture simplification:** replace SRAM + Flash with one memory technology to reduce software management, BOM, board area and qualification effort.

As avionics and other safety-critical platforms migrate from legacy buses to switched Ethernet architectures (ARINC 664/AFDX and related deterministic networks), system performance is increasingly limited not by link speed, but by the ability to store, move and protect data with predictable latency, every time, for the full life of the program. These networks depend on always-valid configuration tables, sustained high-rate packet buffering, and continuous, high-fidelity data capture. In aerospace and spaceflight environments, those same memory structures must also remain intact through power interruptions and radiation exposure.

Everspin *PERSYST* MRAM addresses performance, power, and BOM bottlenecks by collapsing the traditional SRAM + Flash memory hierarchy into a single, high-reliability non-volatile memory that behaves like SRAM while retaining data like Flash, without erase cycles, garbage collection, or wear-out mechanisms. That combination directly maps to the three highest-value insertion points in an ARINC 664 system: **End Systems/AFDX NICs** (Virtual Link descriptor and configuration storage with fast updates), **AFDX switches** (filtering databases and heavy-write packet buffering), and **Flight Data Acquisition Units** (non-volatile cache for "last-gasp" capture up to the instant of power loss).

Just as importantly, the same requirements show up beyond aerospace. Automotive TSN/ISO 26262 and Industrial EtherCAT®/PROFINET IRT designs face the identical need for deterministic response, frequent updates, long mission life and data integrity in electrically harsh environments. By

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standardizing with *PERSYST* MRAM across these platforms, designers can simplify the memory architecture, reduce SWaP-C (size, weight, power and cost) and improve system robustness while maintaining the predictable timing needed for certification and functional safety.

Explore *PERSYST* MRAM for deterministic systems

Learn more about Everspin's xSPI STT-MRAM portfolio for applications requiring persistence, high endurance and predictable performance.

Explore PERSYST MRAM | **Talk with Everspin about your design**

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