Introduction

As embedded systems demand faster access times, higher reliability, and longer operational lifetimes, traditional NOR Flash faces inherent challenges, including erase-before-write requirements, limited program/erase cycle endurance, and relatively slow write performance. Everspin MRAM combines the non-volatility of Flash with the speed and endurance of SRAM, enabling instant writes, high endurance, and simplified memory management. These advantages make MRAM an ideal replacement for NOR Flash in applications that require frequent updates, high system availability, deterministic performance, and long-term data retention.

Beyond its technical benefits, MRAM also provides a qualified alternative to NOR Flash, helping designers reduce supply chain risk while enhancing overall system performance and reliability. For many designs, Everspin MRAM can serve as a direct replacement for NOR Flash, requiring little or no hardware redesign while delivering dramatically faster write performance, higher endurance, and simplified memory management.

This document outlines the key design considerations for migrating from NOR Flash to Everspin MRAM and provides guidance to support a successful transition.

Contents

Interface Compatibility: Protocol, Voltage and Power

Everspin offers two commercially available MRAM technology families, each supporting different interface protocols and operating voltages.

Everspin's first commercial MRAM products were based on its patented Toggle MRAM technology. These devices operate at 3.3V and are available in Parallel x8 and x16 interfaces, as well as legacy Single and Quad SPI interface options.

Everspin's STT MRAM family operates at 1.8V and is xSPI compliant, with support for SPI, Dual SPI, Quad SPI, and Octal SPI modes. These devices support the xSPI Profile 1 command protocol and are intended for higher-performance serial memory applications.

Table 1 summarizes the interface and voltage options available across Everspin's PERSYST MRAM portfolio.

TABLE 1 : TECHNOLOGY INTERFACE AND VOLTAGE

Technology	Interface	Voltage
Toggle MRAM	X8 and X16 Parallel	3.3V
Toggle MRAM	Legacy SPI and QSPI	3.3V
STT MRAM	xSPI: SPI, DSPI, QSPI and Octal	1.8V

If the target system requires interfacing 1.8V STT MRAM to a legacy 3.3V host interface, voltage level shifting or translation will be required. Everspin application note EST3005, level shifter Implementation with EMxxxLX, provides guidance on translator selection and other implementation considerations for this scenario.

After protocol and voltage compatibility have been confirmed, the next consideration is whether the system power architecture can support the selected MRAM device under the intended operating conditions.

Due to the nature of the MRAM cell structure and nanosecond-class write performance, the system 3.3V or 1.8V power supply should be reviewed to ensure it can support the required operating current. For example, Everspin's high-performance PERSYST EMxxxLX devices support up to 200 Mhz DTR write operation. At that performance level, write current can reach 221mA maximum. The associated supply rail must be able to source this current to ensure robust and predictable operation.

In addition to peak active current, the system power budget should also be reviewed for low-power and standby operation. In some applications, standby current may be a key selection criterion, particularly where the legacy memory solution was optimized for very low sleep current. If the target platform does not already provide a 1.8 V rail, the impact of adding a regulator or level-shifting solution should also be included in the system-level power analysis.

Power-fail behavior should also be considered during migration. Because MRAM is non-volatile and does not require erase-before-write operation, it can provide meaningful robustness advantages in systems exposed to unexpected power interruption. Applications that frequently update parameters, logs, or status information may benefit from reduced vulnerability during interrupted write activity compared with erase-based memory technologies. System designers should still validate their update methodology, but MRAM can simplify the design of robust data-retention and recovery strategies.

Temperature selection

Everspin MRAM is available in multiple temperature grades to support a wide range of system operating environments. This flexibility can be an important consideration when migrating from NOR Flash, particularly in applications with industrial, extended temperature, or automotive requirements.

Available temperature grades include:

a) Commercial Grade: 0 °C to 85 °C
b) Industrial Grade: -40 °C to 85 °C
c) Extended Temperature Grade: -40 °C to 105 °C
d) Automotive Grade: -40 °C to 125 °C
e) Automotive AEC-Q100 Grade: -40 °C to 125 °C

When evaluating a replacement device, designers should confirm not only protocol and density compatibility, but also that the selected memory grade aligns with the system's required operating temperature range. Everspin's broad-temperature offering can provide an advantage where alternate solutions do not support the required environmental range or are only available in wider temperature grades than the application actually needs. Selecting the appropriate temperature grade can help avoid unnecessary over-specification and may reduce overall memory cost.

Once interface, voltage, and power considerations have been reviewed, the next step is to evaluate package compatibility and required device density.

Package and device density requirements

Everspin MRAM is available in multiple package and density options. When evaluating a migration path, the lowest-risk approach is often to select a device that matches the existing or planned board footprint as closely as possible, helping minimize layout changes and overall redesign effort.

When migrating from NOR Flash to MRAM, designers should re-evaluate memory density requirements in the context of endurance. NOR Flash-based systems often rely on overprovisioning and wear-leveling algorithms to extend usable lifetime, which can result in selecting higher densities than functionally required. In contrast, MRAM offers extremely high endurance and does not require erase-before-write operations, eliminating the need for wear leveling. As a result, system designers may be able to select a lower density device while still exceeding lifetime requirements, reducing both memory footprint and overall system cost while simplifying software complexity.

Everspin offers several package and density combinations across its supported interface and protocol families. Table 2 summarizes the available package, protocol, and density options to help identify the most practical migration path for a given application.

The range of package and density options can help designers balance migration simplicity, board constraints, and required memory capacity without forcing unnecessary redesign.

TABLE 2 PACKAGES PROTOCOL AND DENSITIES

Package	Protocol	Density
BGA 48, TSOP 44 & 54	x8 and x16 Parallel	256Kb,1,2,4,8,16 and 32Mb
5x6 DFN	Legacy SPI	128Kb, 256Kb, 1Mb, 4Mb
16-SOIC, BGA24	Legacy Quad SPI	1Mb
5x6 DFN	xSPI: SPI, DSPI and QSPI	4, 8 and 16Mb
8x6 DFN, BGA24	xSPI: SPI, DSPI and QSPI	32, 64, 128Mb
BGA24	xSPI: SPI, DSPI, QSPI and Octal	4,8,16,32,64,128 and 256Mb

If system density requirements exceed the capacity of a single available MRAM device, it is common practice to connect multiple slave devices to one master. Device selection is controlled through the CS# signal for each memory device. Figure 1 shows a typical connection scheme for a single SPI master with multiple slave devices. Quad SPI and Octal SPI devices are connected in a similar manner with the corresponding IO[0:3] or IO[0:7] signals from the Host Controller routed to the associated signals of each device.

The number of devices that can be connected depends on the drive capability and loading limits of the selected SPI master. Designers should review the relevant host-controller documentation to confirm that signal integrity, fanout, and timing requirements remain within specification for the intended configuration.

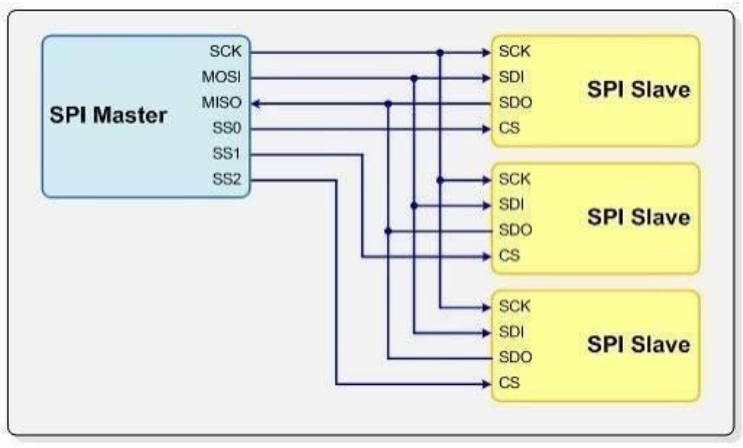

FIGURE 1 MULTIPLE SPI SLAVE CONNECTION SCHEME

When multiple MRAM devices are used to achieve the required density, the design should also account for chip-select decoding, bus loading, timing margin, and boot or initialization behavior. Although this approach can extend usable density beyond a single device, designers should confirm that the host controller, firmware, and board-level signal integrity remain acceptable as additional devices are added.

Where possible, footprint planning should consider not only the immediate migration target, but also longer-term sourcing and revision flexibility. Selecting common package styles and preserving layout options that simplify replacement or second-source evaluation can reduce future redesign effort. If the application is expected to evolve across multiple memory options, evaluating footprint strategy early can help keep future migration paths practical.

High Speed routing considerations for xSPI

With the adoption of the xSPI specification, significantly higher serial-memory interface performance is now available. The current maximum speed supported by the xSPI specification is 200Mhz with DTR (Dual Transfer Rate) operation, enabling data transfer rates of up to 400MB/s. For designs migrating from lower-speed SPI or Quad SPI NOR Flash, these routing and validation considerations become more important when taking full advantage of xSPI performance enabled by Everspin MRAM.

To support reliable operation at these data rates, proper PCB routing and layout practices should be followed. As part of the board-design process, simulation of the proposed interconnect is recommended to evaluate signal integrity and timing margin. Everspin supports customer simulation activities through the availability of IBIS models for its MRAM devices.

IBIS models for Everspin MRAM devices are available on the Everspin website under IBIS Models.

If a new layout is required to support higher xSPI bus speeds, validation and tuning of the bus timing may be required to ensure robust system operation. At the highest bus speeds, optimum receiver timing is determined by tunning the sampling point of the data presented on the bus. To support this process, Everspin provides application note EST3001 Tuning Data Pattern for EMxxLX, which can assist with bus-timing validation and receiver-tuning activities.

Command set compatibility

Command-set compatibility is an important part of any NOR Flash to MRAM migration. Depending on the selected Everspin device and the host-controller implementation, designers should review the supported command set to confirm that the intended read, write, mode-entry, and protocol-selection operations are aligned with system requirements.

- Everspin's MR25Hxx SPI devices support the legacy SPI command set identified in Table 2, Command Codes, of the applicable device data sheet.
- Everspin's MR10Q010 QSPI device supports the legacy SPI command set identified in Table 7, SPI Mode Commands Overview, in addition to the Quad SPI command set identified in Table 9, Quad SPI Mode Commands Overview, of the applicable device data sheet.
- Everspin's EMxxxLX STT-MRAM family supports the full xSPI command set, as identified in Table 21, Command Table, of the applicable device data sheet.

During migration, command-set review should also include any firmware assumptions related to erase operations, page programming, status/configuration register access, and protocol initialization so that software behavior remains aligned with the selected MRAM device. In many cases, MRAM can simplify command handling by eliminating erase-related command flows that are commonly required for NOR Flash.

Software optimizations for MRAM features over NOR Flash

Everspin MRAM devices can provide meaningful performance and software-architecture advantages when compared with NOR Flash. To realize these benefits, designers should review the existing software implementation and identify any legacy assumptions that were originally introduced to accommodate NOR Flash behavior. In many systems, these changes can reduce firmware complexity while also improving response time for frequent update operations.

The items below are not intended to be exhaustive, but they highlight several common software optimizations that can improve performance, reduce complexity, or simplify memory-management overhead when migrating from NOR Flash to MRAM.

1) Eliminate page or sector erase operations prior to writes.
   MRAM does not require erase-before-write operation. Everspin MRAM is a write-in-place non-volatile memory, allowing data to be updated directly without the erase cycles typically associated with NOR Flash. Removing erase operations can reduce software overhead and improve write responsiveness.

2) Remove wear-leveling and bad-block-management algorithms where appropriate.
   MRAM offers extremely high endurance, typically on the order of 10^{14} writes, which can eliminate the need for wear-leveling strategies or bad-block-management schemes commonly used with Flash-based memories. This can simplify software design and reduce management overhead in many applications.

3) Reevaluate page-programming assumptions.
   Page programming is not required for standard MRAM operation because Everspin MRAM is byte-addressable, with a minimum write granularity of one byte. However, if page-program-style behavior is preferred for compatibility with existing software, the EMxxxLX STT-MRAM family can operate in NOR emulation mode, allowing MRAM to emulate NOR-style programming behavior. Additional details on NOR emulation mode are provided in application note EST3003 EMxxLX in NOR Emulation and XIP

Register settings and Device Initialization requirements

The EMxxxLX family of MRAM has a device initialization requirement that should be understood during system design and manufacturing planning to ensure predictable and defined operational behavior. After board reflow, the register and array contents require a one-time device initialization .

This initialization routine sets the required device registers for normal operation and helps ensure that the MRAM is configured appropriately for the intended system-level use model. Designers should account for this step in manufacturing test, board bring-up, or any provisioning flow used to prepare the system for deployment.

The device initialization procedure is described in detail in the application note EST3000, Device Initialization, Reset and Recovery.

It is important to note that initialization/programming of the MRAM devices is required after board assembly. The programming after assembly may differ from the NOR Flash sequence where devices are programmed prior to board assembly. The high speed write capabilities of MRAM devices will allow the initialization/programming to complete in < 2 seconds allowing minimal impact to build cycle timelines.

Conclusion

When evaluating Everspin MRAM as a replacement for NOR Flash, several factors should be reviewed to help ensure proper system functionality, compatibility, and migration readiness. This application note has outlined the primary design considerations involved in that process, including interface selection, power and temperature requirements, package and density planning, command-set review, software implications, and device initialization.

While no single document can address every possible migration scenario, Everspin MRAM can provide meaningful advantages in many applications, including write-in-place operation, high endurance, fast write performance, and expanded temperature-grade options. If additional questions arise for a specific design or migration use case, please contact the Everspin support team at support@everspin.com

Contact Information:

Author: Daniel R. Symalla

Sr. FAE

WW Sales Group

How to Reach Us:

www.everspin.com

E-Mail:

support@everspin.com

orders@everspin.com

sales@everspin.com

USA/Canada/South and Central America

Everspin Technologies

5670 W. Chandler Road, Suite 100

Chandler, Arizona 85226

+1-877-347-MRAM (6726)

+1-480-347-1111

Europe, Middle East and Africa

support.europe@everspin.com

Japan

support.japan@everspin.com

Asia Pacific

support.asia@everspin.com

Everspin Technologies, Inc.