Introduction

This user guide is provided to help users understand the Hardware and Software requirements needed for evaluation of the EMxxLX Industrial STT MRAM device from Everspin.

This guide will outline the Hardware and Software requirements for the user to setup, configure, initialize, and generate traffic test vectors for the EMxxLX device.

This guide assumes the user has full access to the EMxxLX data sheet and a reasonable understanding of HW and SW usage. This guide makes references and links to other support documents for the user.

Contents

List of Figures and Tables

1. EMxxLX Daughter Card

The EMxxLX Daughter Card is populated with Everspin EMxxLX 64Mbit Industrial STT MRAM device. Other EMxxLX densities can be populated as well. This device is obtained through the sample request form on Everspin's website located here:

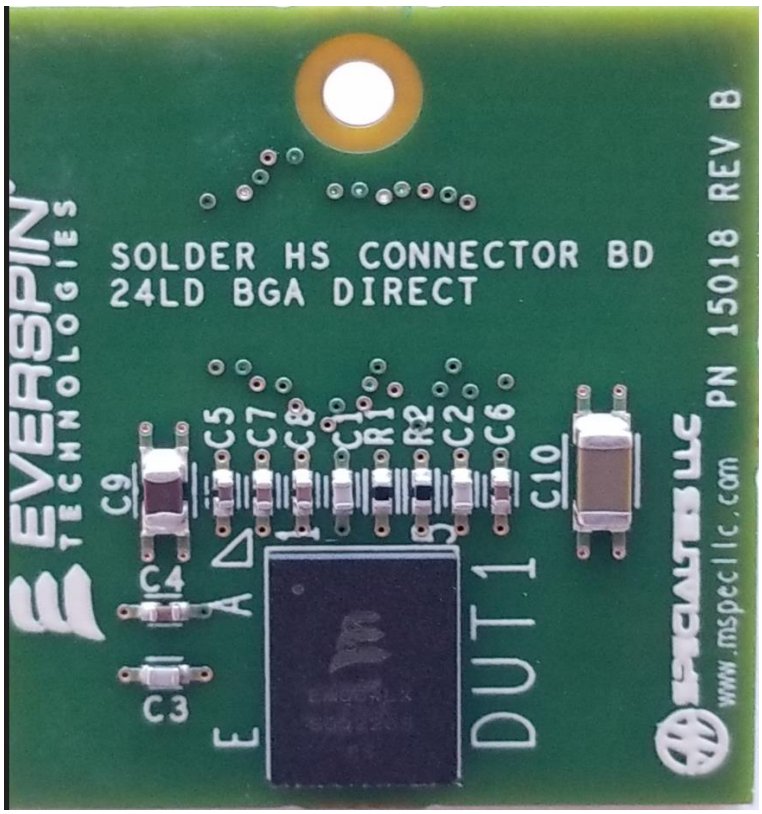

FIGURE 1 EMXXLX DAUGHTER CARD

2. Required Host Board Support

The EMxxLX evaluation board, here in referenced as the EMxxLX daughter card is designed to connect to the Open FPGA specification CRUVI CR00100-01 host board HS (High Speed) slot. This host platform is available to order

from Trenz Electronic LLC website: https://shop.trenz-electronic.de/en/CR00100-01-DBC82A-CRUVI-MAX-10-Base-Board-with-Intel-MAX-10-FPGA-8-MByte-SDRAM-4.5-x-5.7-cm?c=579

The CR00100-01 board has the following key features:

- On Board
  - JTAG and UART over Micro USB connector
  - 2 x User Push button
  - 4 x User LEDs (red, green)
- SoC/FPGA
  - Intel MAX10 FPGA (10M08 as standard option)
- RAM/Storage
  - 8 MByte SDRAM
- Interface
  - 1 x CRUVI LS
  - 1 x CRUVI HS
- Power
  - Power from micro USB connector
- Dimension
  - 44.86 mm x 57.50 mm

FIGURE 2 CRUVI CR00100-01

3. IDE (Integrated Development Environment) Support

The Intel Max10 FPGA is supported using the Intel ® Quartus Prime Lite Edition Design Software. The LITE edition is a free use IDE and is available for download from Intel ® web site located here: https://www.intel.com/content/www/us/en/software-kit/684216/intel-quartus-prime-lite-edition-design-software-version-21-1-for-windows.html

Along with the IDE it is highly encouraged users download the Intel ® recommended documentation.

Documentation Links:

- Intel® Quartus® Prime Software User Guides
- Intel® FPGA Software Installation and Licensing Manual
- Intel® Quartus® Prime Software and Device Support Release Notes (PDF)

4. Memory Controller Support

EMxxLX is Everspin's latest Industrial STT MRAM supporting JESD251 Expanded Serial Peripheral Interface (xSPI). To properly support this new JEDEC standard an xSPI compatible memory controller is required. Synaptic Labs LLC MBMC (Multi-Bus Memory Controller) IP is used in this evaluation board.

The Memory Controller IP is in the Zip file downloaded with this user guide. The Memory controller IP will be installed with the proper license files in section 5 of this user guide.

5. IDE Software Installation and Configuration

To program the FPGA with the correct image Quartus Prime IDE is used in conjunction with Synaptic Labs MBMC (Multi-Bus Memory Controller) IP. Locate the Quartus Prime IDE install file downloaded in section 3. Follow the installation instructions associated with the file. The user guide assumes default file location is used during the installation process.

6. Reference Platform Generation

After installation of the Quartus Prime IDE, Synaptic Memory controller IP and license files require installation. The license file installation and configuration is a detailed and multi-step process.

For detailed installation instructions please refer to the included file: "SLL Multiple Bus Memory Controller (MBMC) IP Installation Guide with Detailed Step-by-Step Instructions"

Follow the Synaptic Labs' Tutorial up through and including Section 6.1. This will configure the Quartus Prime IDE to support the CR00100-01 CRUVI platform, correctly configure the FPGA interfaces and prepare the board for the next steps defined in section 7 below.

Section 6.2-8.0 of the Synaptic Labs' Tutorial guide the user through Compiling and generating an FGPA bit stream (.SOF file) and test program .ELF files. These steps are not required as a precompiled .SOF and .ELF files are provided in CR0010_project_18V_J1_EMLX_Q18p1\Precompiled folder. These files will be loaded in section 7 below.

7. Hardware connection, FPGA Image and .ELF file download

To program the Max10 FPGA a Micro-USB cable with data connection is required. Ensure the cable supports data transfer and not just charging capabilities.

A USB Programmer is required for image download to the FPGA. The arrow USB programmer is used for this task.

The SW and installation instructions are located here:

https://wiki.trenz-electronic.de/display/PD/Arrow+USB+Programmer

After installation of the Arrow USB programmer the CR00100-01 board is ready for the FPGA image download.

Locate the SynapticLabs-Everspin-Bandwidth_Reference_design_CR0010 in the CR0010_project_18V_J1_EMLX_Q18p1\doc folder.

Follow the detailed steps for programming the FPGA bitstream and downloading the .ELF file into CR00100 System SDRAM.

Section 4 of the Reference design document requires the user to use command line options to change the Directory to the **CR0010_project_18V_J1_xxx/precompiled** folder. For users unfamiliar with command line directives in the NIOS2 terminal a good tutorial is located here:

https://johnloomis.org/NiosII/tools/console.html

8. Reading and Writing EMxxLX MRAM

In section 4 of SynapticLabs-Everspin-Bandwidth_Reference_design_CR0010 the user downloaded the .ELF files with contain the workloads for the EMxxLX device.

Follow the command line options to run all predefined workloads provided.

If the user requires specific workload or test vectors, the full project files have been provided. Users can modify the source files located in CR0010_project_18V_J1_EMLX_Q18p1\source_files\emlx_flash_test.

After source file modification, users must recompile and generate new .SOF and .ELF files.

Refer to section 6.2-8.0 of SynapticLabs-xSPI-MBMC-Tutorial001A-NiosII-EMLXTest_CR0010 guide for detailed instructions on .SOF and .ELF generation.

Summary

This Evaluation platform user guide has been provided to give users the ability to evaluate Everspin's EMxxLX Industrial MRAM.

The detailed steps provide users the required download and installation instructions for the Integrated Development Environment (IDE), SW support packages, License files and USB programming tools. After proper configuration, the user can download the required FPGA .SOF and ELF files to test and evaluate EMxxLX industrial MRAM.

Revision History

Revision	Date	Description of change
1.0	October 12, 2022	Initial Release

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