FEATURES 1Gb Non-Volatile ST-DDR4 Spin-transfer Torque MRAM

- 128Mb x8, 64Mb x16 Organization
- Supports most DDR4 features
- Page size of 1024 bits for x8, 2048 bits for x16
- VDD = VDDQ = 1.2v
- VPP = 2.5V
- Operating Temperature of 0˚C to 85 ˚C
- 667MHz clock frequency (fCK)
- On-Device Termination
- Multipurpose register READ and WRITE capability
- Per-Device addressability (PDA)
- Connectivity Test
- On-Chip DLL aligns DQ, DQS, DQS transition with CK transition
- Burst lengths of 8 addresses
- All addresses and control inputs are latched on rising edge of the clock
- Bit Error Rate (BER) = 1 x 10^{-11}
- Data Retention = 3 months at 70°C
- Cycle Endurance = 1 x 10^{10}
- Standard FBGA package options (Pb-free):
- 78-ball (10mm x 13mm) package (x8)
- 96-ball (10mm x 13mm) package (x16)
- Timing – cycle time:
  - 1.5ns @ CL = 10 (ST-DDR4 1333)
  - 1.5ns @ CWL = 9 (ST-DDR4 1333)

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1. CONVENTIONS, DEFINITIONS AND COPYRIGHTS

1.1 Signal Naming Convention

- The terms "_t" and "_c" are used to represent the true and complement of a differential signal pair. These terms replace the previously used notation of "#". For example, differential data strobe pair DQS, DQS# is now referred to as DQS_t, DQS_c.
- The term "_n" is used to represent a signal that is active LOW and replaces the previously used "#" characters. For example: CS# is now referred to as CS_n.
- Addressing is denoted as BG[n] for bank group, BA[n] for bank address, and A[n] for row/col address.

1.2 Device Pin Signal Level

- HIGH: A device pin is driving the logic 1 state.
- LOW: A device pin is driving the logic 0 state.
- High-Z: A device pin is tri-state.
- ODT: A device pin terminates with the ODT setting, which could be terminating or tristate depending on the mode register setting.

1.3 Bus Signal Level

- HIGH: One device on the bus is HIGH, and all other devices on the bus are either ODT or High-Z. The voltage level on the bus is nominally V_{DDQ}.
- LOW: One device on the bus is LOW, and all other devices on the bus are either ODT or High-Z. The voltage level on the bus is nominally V_{OL}(DC) if ODT was enabled, or V_{SSQ} if High-Z.
- High-Z: All devices on the bus are High-Z. The voltage level on the bus is undefined as the bus is floating.
- ODT: At least one device on the bus is ODT, and all others are High-Z. The voltage level on the bus is nominally V_{DDQ}.

2. FUNCTIONAL DESCRIPTION

The ST-DDR4 device (hereafter referred to as “the device”) is a high-speed non-volatile random-access memory internally configured as sixteen banks (4 bank groups with 4 banks for each bank group) for x8 devices, and eight banks for each bank group (2 bank groups with 4 banks each) for x16 devices. The device uses double data rate (DDR) architecture to achieve high-speed operation.

The ST-DDR4 architecture is essentially an 8n prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for a device effectively consists of a single 8n-bit wide, four clock data transfer at the internal ST-DDR4 core and two corresponding one-half clock cycle data transfers at the I/O pins.

Read and write accesses to the device are burst-oriented. Accesses start at a selected location and continue for a burst length of eight or a chopped burst of four in a programmed sequence. Operation begins with the registration of an ACTIVATE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVATE command are used to select the bank and row to be accessed (BG[1:0] select the bank group for x8, and BG0 selects the bank group for x16; BA[1:0] select the bank, and A[15:0] select the row. See “Table 7 - Addressing Scheme” for more details). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst operation, to determine if the auto PRECHARGE command is to be issued (via A10), and select BC4 or BL8 mode on-the-fly (OTF) (via A12) if enabled in the mode register.

Prior to normal operation, the device must be powered up and initialized in a predefined manner.

Refresh operations are not required to maintain data but can optionally be used to move data from the row address buffer to the persistent memory array (store). See REFRESH and SELF - REFRESH command operation.

3. ST-DDR4 SPECIFICATION ENHANCEMENTS, DEVIATIONS & UNSUPPORTED OPTIONS

This section defines the ST-DDR4 MRAM features which are listed as unsupported or deviations or enhancements to JEDEC’s JESD79-4A DDR4 Specification as it pertains to Everspin’s ST-DDR4 persistent memory. ST-DDR4 is DDR4-like, which means it is identical to the AC/DC characteristics and ball/signal assignments to DDR4 memory but varies according to features defined in the Tables 1-3 below. The purpose of this section is to highlight the variations of 1Gb x8, and 1Gb x16 ST-DDR4 MRAM persistent memory devices from JEDEC’s JESD79-4A Specification.

Table 1 - JESD79-4A Specification Enhancements

Feature Description	JEDEC Specification	Everspin Specification
tST – store time	Not Applicable	Store operation period (tST_{min}=380ns). Addressed bank(s) will not be available for a subsequent row activation for a specified time (tST) after the store operation is issued. See "Table 18 – ST-DDR4-1333 Speed Bin Operating Conditions" for more information.
NOMEM mode	MR0[13] is reserved and must be programmed to 0 during MRS	Set MR0[13]=1 to invoke NOMEM before calibration. Reset MR0[13]=0 after calibration is complete. NOMEM mode must be used during calibration to prevent writing over data stored in the persistent memory array. When NOMEM mode is active (MR0[13]=1), data written to the device is only written to the page buffer and not committed to the persistent memory array.
REFRESH	REFRESH	MR3[8] = 1; Refresh command executes a store all banks operation. MR3[8] = 0; disabled, refresh does not perform a store operation. $tRFC_{min}$ must meet tST timing. The store operation can use bank staggering[1] to amortize power usage over time. See the REFRESH command for more information.
SELF-REFRESH	SELF-REFRESH	While in Self-Refresh mode, a store operation will automatically be executed until all data has been moved from all pages in all banks into the persistent memory array. If there are no pages to be stored, the Self-Refresh Command has no effect. $tRFC_{min}$ must meet tST timing. The store operation can use bank staggering[1] to amortize peak power usage over time. See the SELF-REFRESH Operation on page 116 for more information.

[1] See "Table 65 – Bank Staggering Time", MR3[7:6]= 10 (4 banks/update) for x16 devices and 8 banks/update for x8 is the only bank staggering mode supported. Operation proceeds by storing 4 (or 8) banks at a time until all page buffer data has been moved into the persistent memory array. See "Table 18 – ST-DDR4-1333 Speed Bin Operating Conditions" for tST timing

Table 2 - JESD79-4A Specification Deviations

Feature Description	JEDEC Specification	Everspin Specification
x4 DQ	x4, x8, x16 DQ	x8 and x16 DQ only
Speed Bin	-1600, -1866, -2133, -2400	-1333 only (fCK = 667Mhz)
Extended RAS timings: tRCD, tRC, tRAS, tFAW tRP	$tRCD_{min}$ = 12.5ns tRC_{min} = 44.50ns $tRAS_{min}$ =32ns $tFAW_{min}$=15ns tRP_{min} = 12.5ns	$tRCD_{min}$ = 135ns tRC_{min} = 190ns $tRAS_{min}$ = 143ns $tFAW_{min}$ = 240ns tRP_{min} = 7.5ns
CL - CAS Latency	MR0[6:4,2]	MR0[12,6:4,2] = 00001; CL=10 only
CWL - CAS Write Latency	MR2[5:3]	MR2[5:3] = 000; CWL=9 only
Page size	4096b (x4), 8196b (x8), 16,384b (x16)	1024b (x8), 2048b (x16)
tPW_RESET_S - Reset Pulse Width short	tPW_RESET = 1us	tPW_RESET_S = 20uS[1];

[1] Some DRAM vendors have deviated from the JEDEC JESD79-4A Specification and defined short and long versions of tPW_RESET. tPW_RESET = 1uS should now be tPW_RESET_S (short) = 20uS. tPW_RESET_L (long) remains unchanged.

Table 3 - JESD79-4A Unsupported Feature Options

Feature Description	JEDEC Specification	Everspin Specification
Addressing	2Gb, 4Gb, 8Gb, 16Gb RA = A0-A17 CA = A0–A9	1Gb only RA = A0–A15 CA = A0–A6
Command/Address Latency	MR4[8:6]	MR4[8:6] = 000; Disable only
READ Burst Type	MR0[3]	MR0[3] = 0; Sequential only; starting burst CA for BL8 should be CA[2:0]=000; for BC4 CA[1:0] = 00;
Temperature Controlled Refresh	MR4[3]	MR4[3] = 0; Disable only
Fine Granularity Refresh Mode	MR3[8:6]	MR3[8:6] = 010; to set tST, see sec. 12.17
Low power Array Self-Refresh	MR2[7:6]	MR2[7:6] = 00; Manual Mode only (Normal Operating Temperature Range)
Self-Refresh Abort	MR4[9]	MR4[9] = 0; Disable only
MPR Read Data Format	MR3[12:11]	MR3[12:11] = 00; Serial only
MPR Page 1	CA Parity Error Log)	Not defined
Data Bus Inversion	MR5[12:11]	MR5[12:11] = 00; Disable only
Write CRC	MR2[12]	MR2[12] = 0; Disable only
CA Parity	MR5[2:0]	MR5[2:0] = 000; Disable only
Programmable Preamble	MR4[12:11]	MR4[12:11] = 00; 1CK only
Dynamic ODT	MR2[10:9]	MR2[10:9] = 00; Dynamic ODT disabled Use RTT_PARK only (See ODT Impedance Mode below)
Additive Latency	MR1[4:3]	MR1[4:3] = 00; AL Disabled
Gear-down mode	MR3[3]	MR3[3] = 0; 1/2 rate support only
Temperature sensor readout	MR3[5]	MR3[5] = 0; Disable only
hPPR - Post package repair mode	Not in spec[1]	Not applicable to ST-DDR4 MRAM devices
sPPR - Soft post package repair mode	Not in spec[3]	Not applicable to ST-DDR4 MRAM devices

[1] Some DRAM vendors have deviated from the JEDEC JESD79-4A Specification and defined their own parameters.

Feature Description	JEDEC Specification	Everspin Specification
ODT Impedance Mode	MR1[10:8] – RTT_NOM MR5[8:6] – RTT_PARK MR2[10:9] – RTT_WR	MR1[10:8] = 000; RTT_NOM disable only MR5[8:6] = 000 – 111; RTT_PARK supported for disable (000) or impedance range from RZQ/4 – RZQ/7 MR2[11:9][1] = 000; Dynamic ODT Off and RTT_WR disable Of the four impedance states, RTT_PARK, RTT_NOM, RTT_WR and Data Termination Disable, RTT_PARK and Data Termination Disable are the only modes supported.
ZQCS - ZQ Calibration Short	ZQCS command is used to perform periodic calibrations to account for voltage and temperature variations using a shorter amount of time than ZQCL.	The ZQCS command is not supported and is ignored. The standard ST-DDR4 initialization sequence is similar to the DDR4 initialization sequence and should include ZQCL. ZQCL can be issued during normal operation.
Asynchronous ODT timing mode	MR1[0] = 0; DLL off MR1[0] = 1; DLL on	MR1[0] =0; Asynchronous ODT mode is selected when the device runs in DLL-off mode.
MPSM - Max Power Saving Mode	MR4[1]	MR4[1] = 0; Disable only
tCPDED - Command Pass Disable Delay	tCPDED = 4CK	tCPDED = 8CK
tCKSRE - Valid Clock Requirement after Self-Refresh Entry (SRE)	tCKSRE = 5CK	tCKSRE = tST; See tST timing parameter.
tWTR_L - Delay from start of internal write transaction to internal read command for same bank group	max(4CK,7.5ns)	tWTR_L=tWTR_S = min 6CK
tWTR_S - Delay from start of internal write transaction to internal read command for different bank group	max(2CK,2.5ns)	tWTR_L=tWTR_S = min 6CK
Connectivity Test mode: CK_t and CK_c	Upon the assertion of the TEN pin, the CK_t and CK_c signals will be ignored and the DDR4	During CT mode, CK_t and CK_c must always be complementary of each other to maintain differential inputs.

[1] Some memory vendors have deviated from the JEDEC JESD79-4A Specification by including A11 (MR2[11:9]) instead of MR2[10:9]

Feature Description	JEDEC Specification	Everspin Specification
	memory device enter into the CT mode after tBSCAN enable	
Connectivity Test mode: Min Term Equations	MT2 = XOR (A2, A5, A15)	MT2 = XOR (A2, A5, A13)[1]
Connectivity Test Mode: Logic Output Equations	x4, x8, x16	x8, x16 supported See “Table 64 - Connectivity Mode Pin Description and Switching Levels”

[1] Some DRAM vendors have deviated from the JEDEC JESD79-4A Specification and defined their own min term equations. Note: Everspin uses A13 instead of A15 in the MT2 min term equation.

4. SIMPLIFIED STATE DIAGRAM

This simplified state diagram provides an overview of the possible state transitions and the commands to control them. Situations involving more than one bank, the enabling or disabling of on-die termination, and how data is automatically moved from the page buffer into the persistent array (store) and some other events are not captured in full detail.

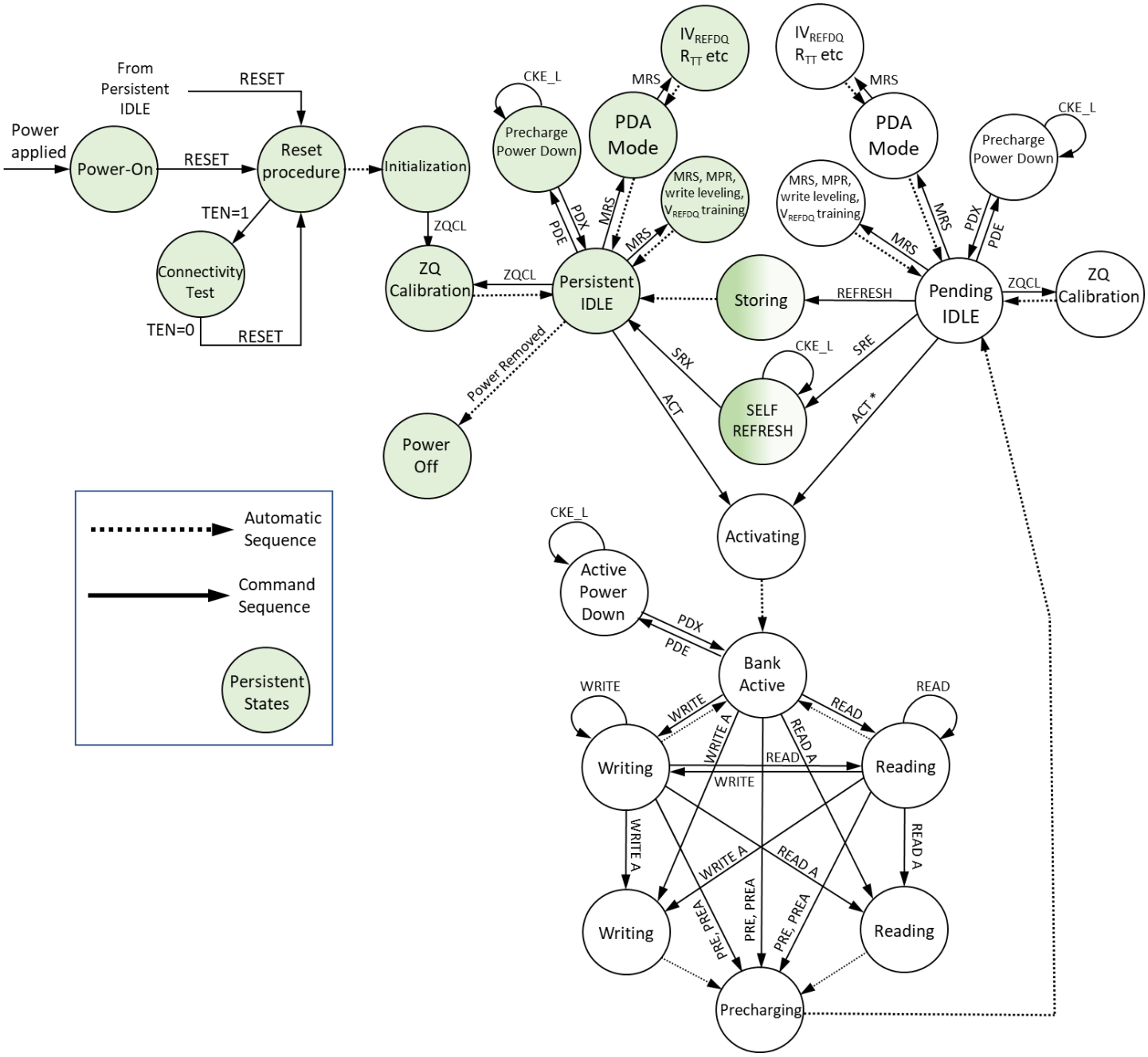

Figure 1 - Simplified State Diagram for ST-DDR4

Table 4 – State Diagram Command Definitions

Command	Description
ACT	Activate
ACT *	Activate with a store operation. When an ACT command is issued from the Pending IDLE state and if a Bank was previously opened, the contents of the page buffer from the previous cycle will automatically be moved into the persistent memory array (store operation) ONLY if the pending access is to a different row within the same bank. This action will guarantee data persistence before overwriting the page buffer during the current cycle. If the pending page access is to a different bank, no automatic store will occur and the Activate will proceed as normal.
MPR	Multipurpose register
MRS	Mode register set
PDE	Enter power-down
PDX	Exit power-down
PRE	Precharge
PREA	Precharge all
READ	RD, RDS4, RDS8
READ A	RDA, RDAS4, RDAS8
REFRESH	Refresh; When the REFRESH command is issued, MR3[8]=1 must be set. When enabled, the Refresh command will move data from each page buffer from each bank into the persistent memory array (store). Fine granularity refresh mode is not supported. See Table 1 - JESD79-4A Specification Enhancements for more details. If MR3[8]=0, the REFRESH command will be ignored and no store all operation will occur.
RESET	Start reset procedure
SRE	Self-Refresh entry; While in Self-Refresh mode the device will automatically move all data from each page buffer in each bank into the persistent memory array. If there are no pages to store, the Self-Refresh command has no effect. $tRFC_{min}$ must meet tST timing.
SRX	Self-Refresh exit; The SRX command will cause a transition from the Self-Refresh state to the Persistent IDLE state.
TEN	Boundary scan mode enable
WRITE	WR, WRS4, WRS8
WRITE A	WRA, WRAS4, WRAS8
ZQCL	ZQ calibration long
ZQCS	ZQ calibration short is not supported

5. FUNCTIONAL BLOCK DIAGRAM

ST-DDR4 MRAM is a high-speed, dynamic random-access persistent memory. It is internally configured as a 16-bank (4-banks per Bank Group) MRAM for the x8 device and 8-bank (2-banks per Bank Group) for the x16 device.

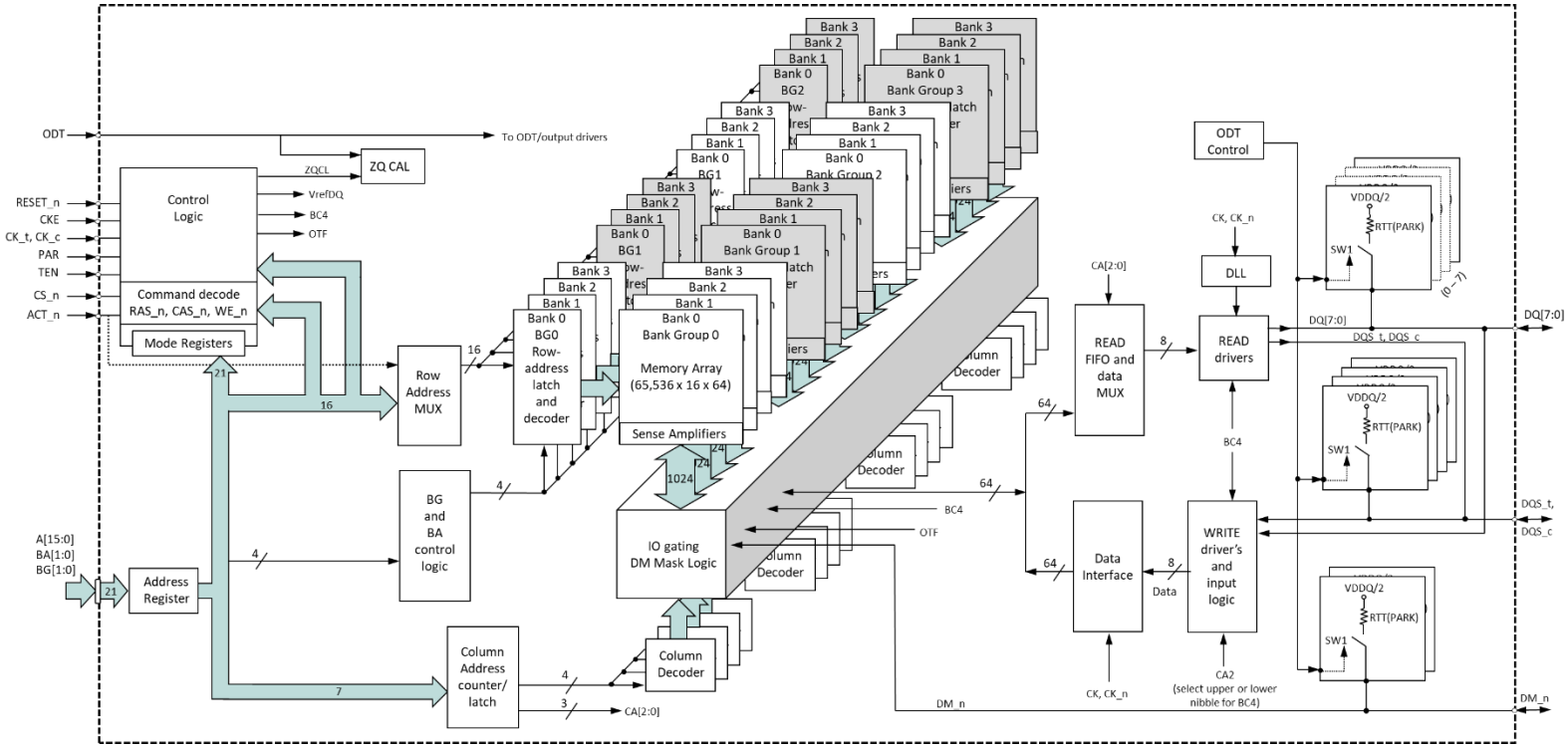

Figure 2 - Functional Block Diagram for 1Gb x8 ST-DDR4

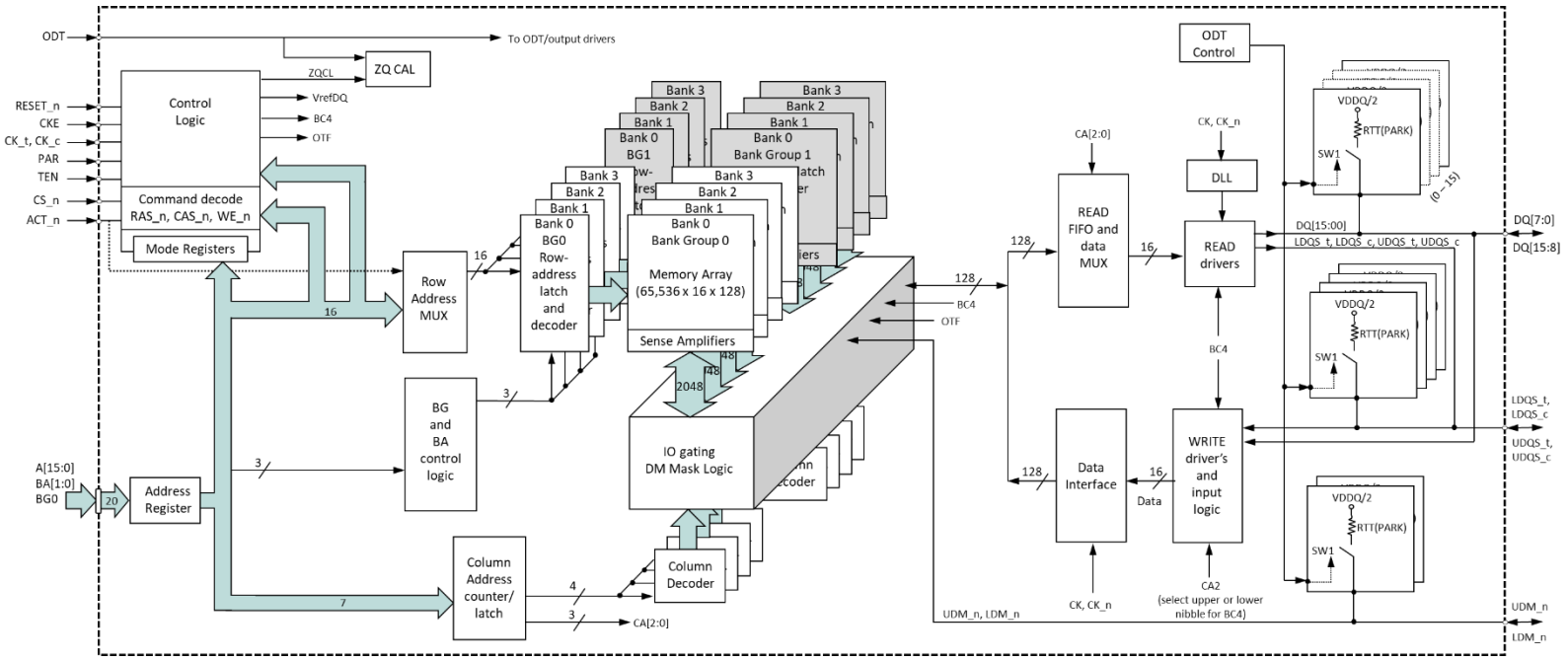

Figure 3 - Functional Block Diagram for 1Gb x16 ST-DDR4

Table 5 - ST-DDR4 Specific Features

Parameter	Description	Limit
Bit Error Rate (BER) Limit to end of life	It is expected that bit errors will be soft and distributed throughout the address space so that the system ECC will correct the errors. BER is after the maximum number of page cycles, or at the end of endurance life.	$1x10^{-11}$
Cycle Endurance	A cycle is defined as a page access and the limit of cycles is for a single page. After this number of cycles in a single page, the bit error rate may start to increase above the BER limit. System level ECC is recommended.	$1x10^{10}$
Data Retention	The data retention time starts from the last read or write cycle and does not differ between powered up and powered down conditions. To maintain data longer than the specified Data Retention time, scrubbing data at a faster rate is required. Please contact Everspin for related application notes.	3 months @ 70°C

5.1 Available Speed Bins

Table 6 – Available Speed Bins

Speed Bin (MT/s)	Orderable Part Number Family	tRCD (ns)	tRP (ns)	CL (ns)
1333	EMD4E001Gxxxx-150	135	7.5	15

5.2 Addressing Scheme

Table 7 - Addressing Scheme

Parameter	128Mb x8	64Mb x16
Number of Bank Groups	4	2
Bank Group Address	BG[1:0]	BG0
Bank Count per Group	4	4
Bank Address in Bank Group	BA[1:0]	BA[1:0]
Row Addressing	64K (A[15:0])	64K (A[15:0])
Column Addressing	128 (A[6:0])	128 (A[6:0])
Page Size[1]	1Kbit	2Kbits

[1] Page size is per bank, calculated as follows: Page size = 2COLBITS x ORG, where COLBITS = the number of column address bits and ORG = the number of DQ bits.

6. PACKAGING and SIGNAL DESCRIPTIONS

The device package ball assignments conform to JESD79-4A Standard DDR4 SDRAM footprints and pin assignments for 78-ball and 96-ball packages.

Table 8 - 78-ball FBGA x8 (top view)

Row	1	2	3	4	5	6	7	8	9	Row
A	V_{DD}	V_{SSQ}	TDQS_c				DM_n / TDQS_t	V_{SSQ}	V_{SS}	A
B	V_{PP}	V_{DDQ}	DQS_c				DQ1	V_{DDQ}	ZQ	B
C	V_{DDQ}	DQ0	DQS_t				V_{DD}	V_{SS}	V_{DDQ}	C
D	V_{SSQ}	DQ4	DQ2				DQ3	DQ5	V_{SSQ}	D
E	V_{SS}	V_{DDQ}	DQ6				DQ7	V_{DDQ}	V_{SS}	E
F	V_{DD}	NC	ODT				CK_t	CK_c	V_{DD}	F
G	V_{SS}	NC	CKE				CS_n	NC	TEN	G
H	V_{DD}	WE_n / A14	ACT_n				CAS_n / A15	RAS_n	V_{SS}	H
J	VREFCA	BG0	A10 / AP				A12 / BC_n	BG1	V_{DD}	J
K	V_{SS}	BA0	A4				A3	BA1	V_{SS}	K
L	RESET_n	A6	A0				A1	A5	ALERT_n	L
M	V_{DD}	A8	A2				A9	A7	V_{PP}	M
N	V_{SS}	A11	PAR				NC	A13	V_{DD}	N
	1	2	3	4	5	6	7	8	9	

Table 9 - 96-ball FBGA x16 (top view)

Row	1	2	3	4	5	6	7	8	9	Row
A	V_{DDQ}	V_{SSQ}	DQ8				DQSU_c	V_{SSQ}	V_{DDQ}	A
B	V_{PP}	V_{SS}	V_{DD}				DQSU_t	DQ9	V_{DD}	B
C	V_{DDQ}	DQ12	DQ10				DQ11	DQ13	V_{SSQ}	C
D	V_{DD}	V_{SSQ}	DQ14				DQ15	V_{SSQ}	V_{DDQ}	D
E	V_{SS}	UDM_n	V_{SSQ}				LDM_n	V_{SSQ}	V_{SS}	E
F	V_{SSQ}	V_{DDQ}	DQSL_c				DQ1	V_{DDQ}	ZQ	F
G	V_{DDQ}	DQ0	DQSL_t				V_{DD}	V_{SS}	V_{DDQ}	G
H	V_{SSQ}	DQ4	DQ2				DQ3	DQ5	V_{SSQ}	H
J	V_{DD}	V_{DDQ}	DQ6				DQ7	V_{DDQ}	V_{DD}	J
K	V_{SS}	CKE	ODT				CK_t	CK_c	V_{SS}	K
L	V_{DD}	WE_n / A14	ACT_n				CS_n	RAS_n	V_{DD}	L
M	V_{REFCA}	BG0	A10 / AP				A12 / BC_n	CAS_n / A15	V_{SS}	M
N	V_{SS}	BA0	A4				A3	BA1	TEN	N
P	RESET_n	A6	A0				A1	A5	ALERT_n	P
R	V_{DD}	A8	A2				A9	A7	V_{PP}	R
T	V_{SS}	A11	PAR				NC	A13	V_{DD}	T
	1	2	3	4	5	6	7	8	9	

Table 10 - Signal Functions and Descriptions

Symbol	Type	Name	Description
A[15:0]	Input	Address Inputs	**Address inputs:** Provide the row address for ACTIVATE commands and the column address for READ/WRITE commands to select one location out of the memory array in the respective bank. (A10/AP, A12/BC_n, WE_n/A14, CAS_n/A15 have additional functions, see other entries in this table.) The address inputs also provide the opcode during the MODE REGISTER SET command.
A10 / AP	Input	Auto Precharge	**Auto-precharge:** A10 is sampled during READ and WRITE commands to determine whether Auto-precharge should be performed to the accessed bank after a READ or WRITE operation. (HIGH = auto precharge; LOW = no auto precharge). A10 is sampled during a PRECHARGE command to determine whether the PRECHARGE applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be

Symbol	Type	Name	Description
			precharged, the bank is selected by the bank group and bank addresses.
A12 / BC_n	Input	Burst chop	**Burst chop:** A12/BC_n is sampled during READ and WRITE commands to determine if burst chop (on-the-fly) will be performed. (HIGH = no burst chop; LOW = burst chopped). See “Table 60 - Command Truth Table”.
ACT_n	Input	Command Input	**Command input:** ACT_n indicates an ACTIVATE command. When ACT_n (along with CS_n) is LOW, the input pins RAS_n, CAS_n/A15, and E_n/A14 are treated as row address inputs for the ACTIVATE command. When ACT_n is HIGH (along with CS_n LOW), the input pins RAS_n, CAS_n/A15, and WE_n/A14 are treated as normal commands that use the RAS_n, CAS_n, and WE_n signals. See “Table 60 - Command Truth Table”.
BA[1:0]	Input	Bank address inputs	**Bank address inputs:** Define the bank (within a bank group) to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. Also determines which mode register is to be accessed during a MODE REGISTER SET command.
BG[1:0]	Input	Bank group address inputs	**Bank group inputs:** Define the bank group to which a REFRESH, ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. BG0 also determines which mode register is to be accessed during a MODE REGISTER SET command. BG[1:0] are used in the x8 configurations. BG1 is not used in the x16 configuration.
CK_t, CK_c	Input	Clock	**Clock:** Differential clock inputs. All address, command, and control input signals are sampled on the crossing of the positive edge of CK_t and the negative edge of CK_c.
CKE	Input	Clock enable	**Clock enable:** CKE HIGH activates and CKE LOW deactivates the internal clock signals, device input buffers, and output drivers. Taking CKE LOW provides Precharge Power-Down and Self-Refresh operations (all banks idle), or Active Power-Down (row active in any bank). CKE is asynchronous for Self-Refresh exit. After V_{REFCA} has become stable during the power-on and initialization sequence, it must be maintained during all operations (including SELF-REFRESH). CKE must be maintained HIGH throughout read and write accesses. Input buffers (excluding CK,_t, CK_c, ODT, RESET_n, and CKE) are disabled during power-down. Input buffers (excluding CKE and RESET_n) are disabled during self-refresh.

Symbol	Type	Name	Description
CS_n	Input	Chip select	**Chip select:** All commands are masked when CS_n is registered HIGH. CS_n provides for external rank selection on systems with multiple ranks. CS_n is considered part of the command code.
DM_n, UDM_n, LDM_n	Input	Input data mask	**Input data mask:** DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a write access. DM_n is sampled on both edges of DQS. The UDM_n and LDM_n pins are used in the x16 configuration: UDM_n is associated with DQ [15:8]; LDM_n is associated with DQ[7:0]. The DM_n, DBI, and TDQS functions are enabled by mode register settings. See the Data Mask section
ODT	Input	On-die termination	**On-die termination:** ODT (registered HIGH) enables termination resistance internal to the ST-DDR4 device. When enabled, ODT (RTT) is applied only to each DQ, DQS_t, DQS_c, DM_n/TDQS_t, and TDQS_c (When TDQS_t is enabled via Mode Register A11=1 in MR1) signals for the x8 configuration. For the x16 configuration, RTT is applied to each DQ, DQSU_t, DQSU_c, DQSL_t, DQSL_c, UDM_n, and LDM_n signal. The ODT pin will be ignored if MR1 is programmed to disable RTT.
PAR	Input	Parity for command and address	**Parity for command and address:** This signal is attached to an input buffer but controls no logic internally.
RAS_n /A16, CAS_n /A15, WE_n /A14	Input	Command inputs	**Command inputs:** RAS_n/A16, CAS_n/A15, and WE_n/A14 (along with CS_n and ACT_n) define the command and/or address being entered. See the ACT_n description in this table.
RESET_n	Input	Active LOW asynchronous reset	**Active LOW asynchronous reset:** Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail-to-rail signal with DC HIGH and LOW at 80% and 20% of V_{DD} (960 mV for DC HIGH and 240 mV for DC LOW).
TEN	Input	Ground	**Connectivity test mode:** TEN is active when HIGH and inactive when LOW. TEN must be LOW during normal operation. HIGH in this pin will enable Connectivity Test

Symbol	Type	Name	Description
			Mode operation along with other pins. TEN is a CMOS rail-to-rail signal with DC HIGH and LOW at 80% and 20% of V_{DD} (960mV for DC HIGH and 240mV for DC LOW).
DQ	I/O	Data input/ output	**Data input/output:** Bidirectional data bus. DQ represents DQ[7:0] and DQ [15:0] for the x8 and x16 configurations, respectively. DQ0 may be used to monitor the internal V_{REF} level during test via mode register setting MR4 A [4] = HIGH, training times change when enabled. During this mode, the R_{TT} value should be set to High-Z. This measurement is for verification purposes and is NOT an external voltage supply pin.
DQS_t, DQS_c, DQSU_t, DQSU_c, DQSL_t, DQSL_c	I/O	Data strobes	**Data strobe:** Output with READ data, input with WRITE data. Edge-aligned with READ data, centered-aligned with WRITE data. For the x16, DQSL corresponds to the data on DQ[7:0]; DQSU corresponds to the data on DQ[15:8]. For the x8 configuration, DQS corresponds to the data on DQ[7:0]. The ST-DDR4 device supports a differential data strobe only and does not support a single-ended data strobe.
ALERT_n	Output	Alert output	**Alert output:** During normal operation this signal is an output and is driven HIGH. During Connectivity Test mode, this pin works as an input.
TDQS_t, TDQS_c	Output	Termination data strobe	**Termination data strobe:** TDQS_t and TDQS_c are used by x8 devices only. When enabled via the mode register, the device will enable the same R_{TT} termination resistance on TDQS_t and TDQS_c that is applied to DQS and DQS. When the TDQS function is disabled via the mode register, the DM/TDQS pin will provide the DATA MASK (DM) function, and the TDQS pin is not used. The TDQS function must be disabled in the mode register for the x16 configuration. The DM function is supported in both x8 and x16 configurations.
NC	-	NC	**No connect:** These balls should be left unconnected (the ball has no connection to the MRAM or to other balls).
VDD	Supply	Power supply	Power supply: 1.2V ±0.06V.
VDDQ	Supply	DQ Power supply	DQ Power supply: 1.2V ±0.06V.
VPP	Supply	MRAM activating power supply	MRAM activating power supply: 2.5V –0.125V/+0.250V.

Symbol	Type	Name	Description
VREFCA	Supply	Reference Voltage	Reference voltage for control, command, and address pins.
VSS	Supply	Ground	Ground
VSSQ	Supply	DQ Ground	DQ Ground
ZQ	Reference	Reference for ZQ Calibration	Reference for ZQ calibration: This ball is tied to an external 240Ω resistor (RZQ), which is tied to VSSQ

Table 11 - Package Thermal Characteristics

Symbol	Parameter	Value	Unit
T_C	Maximum Operating Case Temperature	85	°C
Θ_{JA}	Thermal Resistance Junction to Ambient, 0 mps airflow	38	°C/watt
	Thermal Resistance Junction to Ambient, 3 mps airflow	23	°C/watt
Θ_{JC}	Thermal Resistance Junction to Case	4	°C/watt

7. ELECTRICAL SPECIFICATIONS

7.1 Absolute Maximum Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 12 - Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
VDD[1]	Voltage on VDD pin relative to VSS	- 0.4	1.5	V
VDDQ[7]	Voltage on VDDQ pin relative to VSS	- 0.4	1.5	V
VPP[7,2,3]	Voltage on VPP pin relative to VSS	- 0.4	3.0	V
VIN, VOUT	Voltage on any pin relative to VSS	- 0.4	1.5	V
T_{STG}[4]	Storage temperature	–55	150	°C

[1] VDD and VDDQ must be within 300mV of each other at all times, and VREF must not be greater than 0.6 × VDDQ. When VDD and VDDQ are <500mV, VREF can be ≤300mV. 2.
[2] Storage temperature is the case surface temperature on the center/top side of the ST-DDR4 device. For measurement conditions, please refer to the JESD51-2 standard.
[3] VPP must be equal to or greater than VDD/VDDQ at all times when powered.
[4] Device functionality is not guaranteed if ambient temperature exceeds the maximum TA during operation.

H_{max}	Maximum magnetic field during read, write, standby or power off.	-	2,000	A/m

7.2 Operating Temperature Range

Operating temperature, T_{OPER}, is the case surface temperature on the center/top side of the ST-DDR4 device. For measurement conditions, refer to the JEDEC document JESD51-2.

Table 13 - Operating Temperature Range

Symbol	Parameter	Min	Max	Unit
T_{OPER}[1]	Normal operating temperature range	0	85	°C

7.3 AC/DC OPERATING CONDITIONS

DC Characteristics are defined under standard measurement conditions specified in JEDEC Standard JESD79-4A.

Table 14 – Recommended Supply Operating Conditions

All voltages referenced to VSS

Symbol	Parameter	Min	Nom	Max	Unit
V_{DD}[2,3,4,5]	Supply Voltage	1.14	1.2	1.26	V
V_{DDQ}[5,6]	I/O supply voltage	1.14	1.2	1.26	V
V_{PP}	Wordline Supply Voltage	2.375	2.5	2.750	V

Table 15 – Slew Rate

Symbol	Parameter	Min	Nom	Max	Unit
V_{DD_SL}[6,7]	Slew Rate	0.004	-	600	V/ms

[1] The normal temperature range specifies the temperatures at which the ST-DDR4 specifications will be supported. During operation, the device case temperature must be maintained between 0°C to 85°C under all operating conditions

[2] Under all conditions VDDQ must be less than or equal to VDD.

[3] VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.

[4] VDD slew rate between 300mV and 80% of VDD, min shall be between 0.004 V/ms and 600V/ms, 20 MHz band-limited measurement.

[5] VDD ramp time from 300mV to VDD, min shall be no longer than 200ms.

[6] Measurement made between 300mV and 80% VDD (minimum level).

[7] The DC bandwidth is limited to 20 MHz.

VDD_ON[1]	Ramp	-	-	200	ms

Table 16 – Leakage

Symbol	Parameter	Min	Max	Unit
Input leakage (excluding ZQ and TEN)[2]	IIN	-2	2	µA
ZQ leakage[4]	IZQ	-3	3	µA
TEN leakage[4,3]	ITEN	-6	6	µA
VREFCA leakage[4]	IVREFCA	-2	2	µA
Output leakage: $V_{OUT} = V_{DDQ}$[5]	IOZpd	-	5	µA
Output leakage: $V_{OUT} = V_{SSQ}$[7,6]	IOZpu	-50	-	µA

7.4 VREFCA Supply

V_{REFCA} is to be supplied to the device and equal to $V_{DD}/2$. The V_{REFCA} is a reference supply input and therefore does not draw biasing current.

The DC-tolerance limits and AC-noise limits for the reference voltages V_{REFCA} are illustrated in the figure below. The figure shows a valid reference voltage $V_{REF(t)}$ as a function of time (V_{REF} stands for V_{REFCA}). $V_{REF(DC)}$ is the linear average of $V_{REF(t)}$ over a very long period of time (1 second). This average has to meet the MIN/MAX requirements. Furthermore, $V_{REF(t)}$ may temporarily deviate from $V_{REF(DC)}$ by no more than $\pm 1\%\ V_{DD}$ for the AC-noise limit.

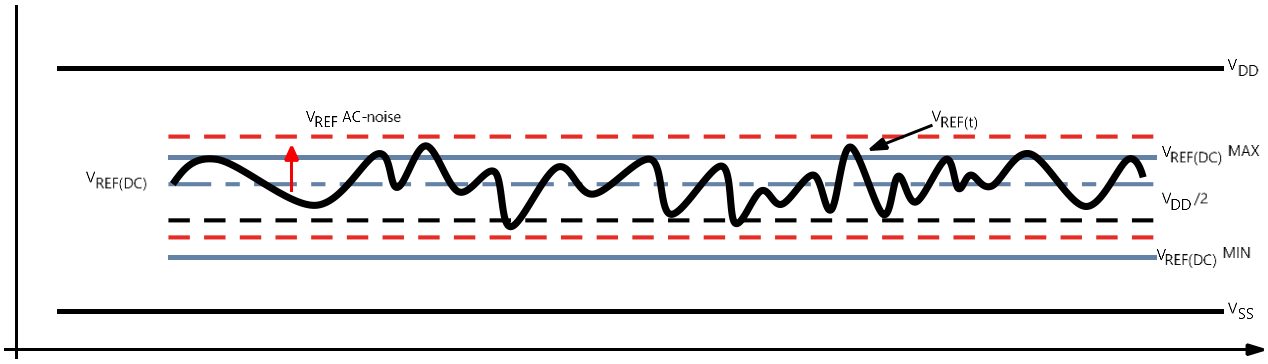

Figure 4 - VREFCA Voltage Range

[1] Maximum time to ramp VDD from 300 mV to VDD minimum.
[2] Input under test 0V < VIN < 1.1V.
[3] Additional leakage due to weak pull-down
[4] VREFCA = VDD/2, VDD at valid level
[5] DQs are disabled
[6] ODT is disabled with the ODT input HIGH

The voltage levels for setup and hold time measurements are dependent on V_{REF}. V_{REF} is understood as VREF(DC), as defined in the above figure. This clarifies that DC-variations of VREF affect the absolute voltage a signal has to reach to achieve a valid HIGH or LOW level, and therefore, the time to which setup and hold is measured. System timing and voltage budgets need to account for $V_{REF(DC)}$ deviations from the optimum position within the data-eye of the input signals. This also clarifies that the device setup/hold specification and derating values need to include time and voltage associated with V_{REF} AC-noise. Timing and voltage effects due to AC-noise on V_{REF} up to the specified limit (±1% of V_{DD}) are included in the device timings and their associated deratings.

7.5 V_{REFDQ} Supply and Calibration Ranges

The device internally generates its own V_{REFDQ}. ST-DDR4 internal V_{REFDQ} specification parameters: voltage range, step size, VREF step time, VREF full step time, and VREF valid level are used to help provide estimated values for the internal V_{REFDQ} and are not pass/fail limits. The voltage operating range specifies the minimum required range for ST-DDR4 devices. The minimum range is defined by $V_{REFDQ,min}$ and $V_{REFDQ,max}$. A calibration sequence must be performed by the ST-DDR4 controller to adjust V_{REFDQ} and optimize the timing and voltage margin of the devices' data input receivers.

7.6 VREFDQ Ranges

MR6[6] selects range 1 (60% to 92.5% of VDDQ) or range 2 (45% to 77.5% of VDDQ), and MR6[5:0] sets the VREFDQ level, as listed in Table 17 - V_{REFDQ} Supply and Calibration Ranges. The values in MR6[6:0] will update the VDDQ range and level independent of MR6[7] setting.

Table 17 - V_{REFDQ} Supply and Calibration Ranges

Symbol	Parameter	Min	Typ	Max	Unit
Range 1 V_{REFDQ} operating points[1,2]	VREFDQ R1	60%	–	92%	VDDQ
Range 2 V_{REFDQ} operating points[1,2]	VREFDQ R2	45%	–	77%	VDDQ
V_{REF} step size[3]	VREF, step	0.5%	0.65%	0.8%	VDDQ
V_{REF} set tolerance	VREF, set_tol	–1.625%	0%	1.625%	VDDQ[4,5,6]
		–0.15%	0%	0.15%	VDD[7,8]
V_{REF} step time[9,10]	VREF, time	–	–	150	ns
V_{REF} valid tolerance[11]	VREF_val_tol	–0.15%	0%	0.15%	VDDQ

[1] VREF(DC) voltage is referenced to VDDQ(DC). VDDQ(DC) is 1.2V
[2] ST-DDR4 range 1 or range 2 is set by the MRS6[A6].
[3] VREF step size increment/decrement range. VREF at DC level
[4] For n > 4, the minimum value of VREF setting tolerance = VREF,new - 1.625% × VDDQ. The maximum value of VREF setting tolerance = VREF,new + 1.625% × VDDQ
[5] Measured by recording the MIN and MAX values of the VREF output over the range, drawing a straight line between those points, and comparing all other VREF output settings to that line.
[6] For n ≤ 4, the minimum value of VREF setting tolerance = VREF,new - 0.15% × VDDQ. The maximum value of VREF setting tolerance = VREF,new + 0.15% × VDDQ
[7] Measured by recording the MIN and MAX values of the VREF output across four consecutive steps (n = 4), drawing a straight line between those points, and comparing all VREF output settings to that line
[8] VREF,new = VREF,old ±n × VREF,step; n = number of steps. If increment, use "+," if decrement, use "-."
[9] Time from MRS command to increment or decrement more than one step size up to the full range of VREF
[10] If the VREF monitor is enabled, VREF,time must be derated by +10ns if DQ bus load is 0pF and an additional +15 ns/pF of DQ bus loading
[11] Only applicable for ST-DDR4 component-level test/characterization purposes. Not applicable for normal mode of operation. VREF valid qualifies the step times, which will be characterized at the component level

7.7 SPEED BIN OPERATING CONDITIONS

Table 18 – ST-DDR4-1333 Speed Bin Operating Conditions

ST-DDR4-1333 Speed Bin				-150		Unit
Parameter		Symbol	Org	Min	Max	
Internal READ command to first data		tAA	x8/x16	15	18	ns
ACT to internal read or write delay time		tRCD	x8/x16	135	-	ns
PRE command period		tRP	x8/x16	7.5	-	ns
Store Operation period		tST	x8/x16	380[1]	-	ns
ACT to PRE command period		tRAS	x8/x16	143	-	ns
ACT to ACT or REF command period		tRC	x8/x16	190	-	ns
Four activate window		tFAW[1]	x8/x16	240	-	ns
READ	WRITE	Symbol	Org	Min	Max	Unit
CL = 10	CWL = 9	tCK(AVG)	x8/x16	1.5	1.6	ns
Supported CL settings				10		CK
Supported CWL settings				9		CK

[1] See ”Table 65 – Bank Staggering Time”

8. I_{DD}, I_{PP} AND I_{DDQ} SPECIFICATION PARAMETERS

IDD and IPP values are for full operating range of voltage and temperature unless otherwise noted.

Table 19 - I_{DD}, I_{PP} and I_{DDQ} Current Limits (mA)

Symbol	ST-DDR4-1333 (x8)		ST-DDR4-1333 (x16)	
	Typ	Max	Typ	Max
I_{DD0}: One bank ACTIVATE-to-PRECHARGE current	282	345	437	500
I_{PP0}: One bank ACTIVATE-to-PRECHARGE I_{PP} current[1]	25	35	25	35
I_{DD1}: One bank ACTIVATE-to-READ-to-PRECHARGE current	299	370	460	525
I_{DD2N}: Precharge standby current[2,3]	90	120	90	120
I_{DD2NT}: Precharge standby ODT current	95	120	95	120
I_{DDQ2NT}: Precharge Standby ODT IDDQ Current	20	35	50	60
I_{DD2P}: Precharge power-down current	15	30	15	30
I_{DD2Q}: Precharge quiet standby current	90	120	90	120
I_{DD3N}: Active standby current	95	120	95	120
I_{DD3P}: Active power-down current	15	30	15	30
I_{DD4R}: Burst read current	170	240	180	240
I_{DDQ4R}: Burst read I_{DDQ} current	10	30	20	30
$I_{DD4W:}$ Burst write current	220	290	230	290
I_{DD6N}: Self-Refresh Current: Normal Temperature Range	15	30	15	30
I_{PP6N}: Self-Refresh IPP Current: Normal Temperature Range	10	15	10	15
I_{DD7}: Bank interleave read current	518	610	863	1,030
I_{PP7}: Bank interleave read IPP current	35	50	35	50

8.1 Current Specifications – Patterns and Test Conditions

Before writing software to make IDDx current measurements, understanding how persistent memory operates will be vital to insure the most accurate results. Refer to Figure 1 - Simplified State Diagram for ST-DDR4. The state diagram introduces a store function that occurs automatically in ST-DDR4 when the ACT command is issued from the Pending IDLE state. It's

[1] IPP0 test and limit is applicable for IDD0 and IDD1 conditions.
[2] When DLL is disabled for IDD2N, current changes by approximately - TBD%.
[3] When CAL is enabled for IDD2N, current changes by approximately - TBD%.

called “Activate with a store operation” or ACT * (See Table 4 – State Diagram Command Definitions). When an ACT command is issued from the Pending IDLE state and if a Bank was previously opened, the contents of the page buffer from the previous cycle will automatically be moved into the persistent memory array (store operation) ONLY if the pending access is to a different row within the same bank. This action will guarantee data persistence before overwriting the page buffer during the current cycle. If the current page access is to a different bank, no automatic store will occur and the Activate will proceed as normal. Refer to “Figure 1 - Simplified State Diagram for ST-DDR4” for additional context.

In order to ensure the most accurate results, IDD0/IPP0, IDD1/IPP1, & IDD7 current measurement tables that follow need to add a two write setup to each of the above test procedures to guarantee that every ACT command will cause an automatic store operation to occur. This means the test must alternate between two different addresses[1] within the same bank to guarantee the contents of the page buffer is always evicted and stored into the persistent memory array with each subsequent ACT command.

If an ACT command is issued to another bank, the contents of the current bank will continue to reside in that bank’s volatile page buffer and no store operation will occur. Looping over the same address or alternating to an address in another bank will not cause an automatic store operation to occur and result in a flawed power measurement.

The contents of a page buffer will remain intact until either power is removed from the device, and data in the volatile page buffer will be lost or an ACT to the current bank will automatically force a store operation and move the page buffer contents into the persistent memory array.

Once the two-row write procedure is setup before each of the IDD0/IPP0, IDD1/IPPI & IDD7 tests, each test can be run continuously, alternating between each address[1] in the same bank to measure an accurate time averaged current. The two-row write procedure is embedded into each of the IDD0, IDD1, and IDD7 test measurement tables below.

[1] The two addresses within the same bank used to alternate to guarantee an automatic store with each ACT command are A[15:00]=0x0000 and A[15:00]=0x03F8

Table 20 - IDD0 and IPP0 Measurement-Loop Pattern[1]

CK_t /CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/ A16	CAS_n/ A15	WE_n/ A14	ODT	BG[1:0][2]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[3]
Toggling	Static High	1	0	ACT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		A	1,2	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	
			3,4	D_#, D_#	1	1	1	1	1	0	3	3	0	0	0	7	F	0	
			…	repeat pattern 1...4 until nRCD - 1, truncate if necessary															
			nRCD	WR	0	1	1	0	0	1	0	0	0	0	0	0	0	0	
			…																
			nRAS	PRE	0	1	0	1	0	0	0	0	0	0	0	0	0	0	
			…	repeat pattern 1...4 until nRC-1, truncate if necessary															
		2	nRC	ACT	0	0	0	0	0	0	0	0	0	0	7	F	0	0	
		A	nRC + 1, 2	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	
			nRC + 3, 4	D_#, D_#	1	1	1	1	1	0	3	0	0	0	7	F	0	0	
			…	repeat pattern nRC+1...4 until nRC + nRCD - 1, truncate if necessary															
			nRC + nRCD	WR	0	1	1	0	0	1	0	0	0	0	0	0	0	0	
			…	repeat pattern 1...4 until nRC+nRCD +nRAS- 1, truncate if necessary															
			nRC+nRAS	PRE	0	1	0	1	0	0	0	0	0	0	0	0	0	0	
			…	repeat pattern 1...4 until 2*nRC - 1, truncate if necessary															
		3	2*nRC	Repeat subloop 1A, use BG[1:0]=1, use BA[1:0]=1 instead (bank 5)															
		A	3*nRC	Repeat subloop 2A, use BG[1:0]=1, use BA[1:0]=1 instead (bank 5)															
			4*nRC	Repeat subloop 1A, use BG[1:0]=0, use BA[1:0]=2 instead (bank 2)															
			5*nRC	Repeat subloop 2A, use BG[1:0]=0, use BA[1:0]=2 instead (bank 2)															
			6*nRC	Repeat subloop 1A, use BG[1:0]=1, use BA[1:0]=3 instead (bank 7)															
			7*nRC	Repeat subloop 2A, use BG[1:0]=1, use BA[1:0]=3 instead (bank 7)															
			8*nRC	Repeat subloop 1A, use BG[1:0]=0, use BA[1:0]=1 instead (bank 1)															
			9*nRC	Repeat subloop 2A, use BG[1:0]=0, use BA[1:0]=1 instead (bank 1)															
			10*nRC	Repeat subloop 1A, use BG[1:0]=1, use BA[1:0]=2 instead (bank 6)															
			11*nRC	Repeat subloop 2A, use BG[1:0]=1, use BA[1:0]=2 instead (bank 6)															
			12*nRC	Repeat subloop 1A, use BG[1:0]=0, use BA[1:0]=3 instead (bank 3)															
			13*nRC	Repeat subloop 2A, use BG[1:0]=0, use BA[1:0]=3 instead (bank 3)															
			14*nRC	Repeat subloop 1A, use BG[1:0]=1, use BA[1:0]=0 instead (bank 4)															

[1] DQS_t, DQS_c are VDDQ
[2] BG1 is don't care for x16 device
[3] DQ signals are VDDQ.

CK_t /CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/ A16	CAS_n/ A15	WE_n/ A14	ODT	BG[1:0][2]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[3]
			15*nRC	Repeat subloop 2A, use BG[1:0]=1, use BA[1:0]=0 instead (bank 4)															
			16*nRC	Repeat subloop 1A, use BG[1:0]=2, use BA[1:0]=0 instead (bank 8)															
			17*nRC	Repeat subloop 2A, use BG[1:0]=2, use BA[1:0]=0 instead (bank 8)															
			18*nRC	Repeat subloop 1A, use BG[1:0]=3, use BA[1:0]=1 instead (bank 13)															
			19*nRC	Repeat subloop 2A, use BG[1:0]=3, use BA[1:0]=1 instead (bank 13)															
			20*nRC	Repeat subloop 1A, use BG[1:0]=2, use BA[1:0]=2 instead (bank 10)															
			21*nRC	Repeat subloop 2A, use BG[1:0]=2, use BA[1:0]=2 instead (bank 10)															
			22*nRC	Repeat subloop 1A, use BG[1:0]=3, use BA[1:0]=3 instead (bank 15)															
			23*nRC	Repeat subloop 2A, use BG[1:0]=3, use BA[1:0]=3 instead (bank 15)															
			24*nRC	Repeat subloop 1A, use BG[1:0]=2, use BA[1:0]=1 instead (bank 9)															
			25*nRC	Repeat subloop 2A, use BG[1:0]=2, use BA[1:0]=1 instead (bank 9)															
			26*nRC	Repeat subloop 1A, use BG[1:0]=3, use BA[1:0]=2 instead (bank 14)															
			27*nRC	Repeat subloop 2A, use BG[1:0]=3, use BA[1:0]=2 instead (bank 14)															
			28*nRC	Repeat subloop 1A, use BG[1:0]=2, use BA[1:0]=3 instead (bank 11)															
			29*nRC	Repeat subloop 2A, use BG[1:0]=2, use BA[1:0]=3 instead (bank 11)															
			30*nRC	Repeat subloop 1A, use BG[1:0]=3, use BA[1:0]=0 instead (bank 12)															
			31*nRC	Repeat subloop 2A, use BG[1:0]=3, use BA[1:0]=0 instead (bank 12)															
		0	32*nRC	ACT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			32*nRC + 1,2	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			32*nRC + 3,4	D_#, D_#	1	1	1	1	1	0	3[3]	3	0	0	0	7	F	0	-
			…	repeat pattern 1...4 until 32*nRC + nRAS - 1, truncate if necessary															
			32*nRC + nRAS	PRE	0	1	0	1	0	0	0	0	0	0	0	0	0	0	-
			…	repeat pattern 1...4 until nRAS - 1, truncate if necessary															
		1	32*nRC + 1*nRC	repeat Sub-Loop 0, use BG[1:0][3] = 1, BA[1:0] = 1 instead															
		2	32*nRC + 2*nRC	repeat Sub-Loop 0, use BG[1:0][3] = 0, BA[1:0] = 2 instead															
		3	32*nRC + 3*nRC	repeat Sub-Loop 0, use BG[1:0][3] = 1, BA[1:0] = 3 instead															
		4	32*nRC + 4*nRC	repeat Sub-Loop 0, use BG[1:0][3] = 0, BA[1:0] = 1 instead															
		5	32*nRC + 5*nRC	repeat Sub-Loop 0, use BG[1:0][3] = 1, BA[1:0] = 2 instead															
		6	32*nRC + 6*nRC	repeat Sub-Loop 0, use BG[1:0][3] = 0, BA[1:0] = 3 instead															
		7	32*nRC + 7*nRC	repeat Sub-Loop 0, use BG[1:0][3] = 1, BA[1:0] = 0 instead															

CK_t /CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/ A16	CAS_n/ A15	WE_n/ A14	ODT	BG[1:0][2]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[3]
		8	32*nRC + 8*nRC	repeat Sub-Loop 0, use BG[1:0][3] = 2, BA[1:0] = 0 instead[1]															
		9	32*nRC + 9*nRC	repeat Sub-Loop 0, use BG[1:0][3] = 3, BA[1:0] = 1 instead[1]															
		10	32*nRC + 10*nRC	repeat Sub-Loop 0, use BG[1:0][3] = 2, BA[1:0] = 2 instead[1]															
		11	32*nRC + 11*nRC	repeat Sub-Loop 0, use BG[1:0][3] = 3, BA[1:0] = 3 instead[1]															
		12	32*nRC + 12*nRC	repeat Sub-Loop 0, use BG[1:0][3] = 2, BA[1:0] = 1 instead[1]															
		13	32*nRC + 13*nRC	repeat Sub-Loop 0, use BG[1:0][3] = 3, BA[1:0] = 2 instead[1]															
		14	32*nRC + 14*nRC	repeat Sub-Loop 0, use BG[1:0][3] = 2, BA[1:0] = 3 instead[1]															
		15	32*nRC + 15*nRC	repeat Sub-Loop 0, use BG[1:0][3] = 3, BA[1:0] = 0 instead[1]															

[1] For x8 devices only

Table 21 – IDD1 and IPP1 Measurement-Loop Pattern[1,2]

CK_t /CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/ A16	CAS_n/ A15	WE_n/ A14	ODT	BG[1:0][3]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
Toggling	Static High	1A	0	ACT	-	0	0	0	0	0	0	0	0	0	0	0	0	0	
			1,2	D, D	-	0	0	0	0	0	0	0	0	0	0	0	0	0	
			3,4	D_#, D_#	-	1	1	1	1	0	3	3	0	0	0	7	F	0	
			…	repeat pattern 1...4 until nRCD - 1, truncate if necessary															-
			nRCD	WR	-	1	1	0	0	1	0	0	0	0	0	0	0	0	
			…		-														
			nRAS	PRE	-	1	0	1	0	0	0	0	0	0	0	0	0	0	
			…	repeat pattern 1...4 until nRC-1, truncate if necessary															-
		2A	nRC	ACT	-	0	0	0	0	0	0	0	0	0	7	F	0	0	
			nRC + 1, 2	D, D	-	0	0	0	0	0	0	0	0	0	0	0	0	0	
			nRC + 3, 4	D_#, D_#	-	1	1	1	1	0	3	0	0	0	7	F	0	0	
			…	repeat pattern nRC+1...4 until nRC + nRCD - 1, truncate if necessary															-
			nRC + nRCD	WR	-	1	1	0	0	1	0	0	0	0	0	0	0	0	
			…	repeat pattern 1...4 until nRC+nRCD +nRAS- 1, truncate if necessary															-
			nRC+nRAS	PRE	-	1	0	1	0	0	0	0	0	0	0	0	0	0	
			…	repeat pattern 1...4 until 2*nRC - 1, truncate if necessary															-
			2*nRC	Repeat subloop 1A, use BG[1:0]=1, use BA[1:0]=1 instead (bank 5)															-
			3*nRC	Repeat subloop 2A, use BG[1:0]=1, use BA[1:0]=1 instead (bank 5)															-
			4*nRC	Repeat subloop 1A, use BG[1:0]=0, use BA[1:0]=2 instead (bank 2)															-
			5*nRC	Repeat subloop 2A, use BG[1:0]=0, use BA[1:0]=2 instead (bank 2)															-
			6*nRC	Repeat subloop 1A, use BG[1:0]=1, use BA[1:0]=3 instead (bank 7)															-
			7*nRC	Repeat subloop 2A, use BG[1:0]=1, use BA[1:0]=3 instead (bank 7)															-
			8*nRC	Repeat subloop 1A, use BG[1:0]=0, use BA[1:0]=1 instead (bank 1)															-
			9*nRC	Repeat subloop 2A, use BG[1:0]=0, use BA[1:0]=1 instead (bank 1)															-
			10*nRC	Repeat subloop 1A, use BG[1:0]=1, use BA[1:0]=2 instead (bank 6)															-
			11*nRC	Repeat subloop 2A, use BG[1:0]=1, use BA[1:0]=2 instead (bank 6)															-
			12*nRC	Repeat subloop 1A, use BG[1:0]=0, use BA[1:0]=3 instead (bank 3)															-
			13*nRC	Repeat subloop 2A, use BG[1:0]=0, use BA[1:0]=3 instead (bank 3)															-

[1] DQS_t, DQS_c are VDDQ

[2] Before running this test make sure the two write procedure has been correctly implemented. See "**Error! Reference source not found.**". Each test loop is required to alternate between two addresses, A[15:00]=0x0000 and A[15:00]=0x03F8 during ACT to ensure accurate current measurements.

[3] BG1 is don't care for x16 device

[4] Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are VDDQ.

			14*nRC	Repeat subloop 1A, use BG[1:0]=1, use BA[1:0]=0 instead (bank 4)													-
			15*nRC	Repeat subloop 2A, use BG[1:0]=1, use BA[1:0]=0 instead (bank 4)													-
			16*nRC	Repeat subloop 1A, use BG[1:0]=2, use BA[1:0]=0 instead (bank 8)													-
			17*nRC	Repeat subloop 2A, use BG[1:0]=2, use BA[1:0]=0 instead (bank 8)													-
			18*nRC	Repeat subloop 1A, use BG[1:0]=3, use BA[1:0]=1 instead (bank 13)													-
			19*nRC	Repeat subloop 2A, use BG[1:0]=3, use BA[1:0]=1 instead (bank 13)													-
			20*nRC	Repeat subloop 1A, use BG[1:0]=2, use BA[1:0]=2 instead (bank 10)													-
			21*nRC	Repeat subloop 2A, use BG[1:0]=2, use BA[1:0]=2 instead (bank 10)													-
			22*nRC	Repeat subloop 1A, use BG[1:0]=3, use BA[1:0]=3 instead (bank 15)													-
			23*nRC	Repeat subloop 2A, use BG[1:0]=3, use BA[1:0]=3 instead (bank 15)													-
			24*nRC	Repeat subloop 1A, use BG[1:0]=2, use BA[1:0]=1 instead (bank 9)													-
			25*nRC	Repeat subloop 2A, use BG[1:0]=2, use BA[1:0]=1 instead (bank 9)													-
			26*nRC	Repeat subloop 1A, use BG[1:0]=3, use BA[1:0]=2 instead (bank 14)													-
			27*nRC	Repeat subloop 2A, use BG[1:0]=3, use BA[1:0]=2 instead (bank 14)													-
			28*nRC	Repeat subloop 1A, use BG[1:0]=2, use BA[1:0]=3 instead (bank 11)													-
			29*nRC	Repeat subloop 2A, use BG[1:0]=2, use BA[1:0]=3 instead (bank 11)													-
			30*nRC	Repeat subloop 1A, use BG[1:0]=3, use BA[1:0]=0 instead (bank 12)													-
			31*nRC	Repeat subloop 2A, use BG[1:0]=3, use BA[1:0]=0 instead (bank 12)													-
		0	32*nRC	ACT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			32*nRC + 1,2	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			32*nRC + 3,4	D_n, D_n	1	1	1	1	1	0	3	3	0	0	0	7	F	0	-
			…	Repeat pattern 1...4 until 32*nRC + nRCD - AL - 1; truncate if necessary															
			32*nRC + nRCD - AL	RD	0	1	1	0	1	0	0	0	0	0	0	0	0	0	D0=69, D1=69 D2=69, D3=69 D4=69, D5=69 D6=69, D7=69
			…	Repeat pattern 1...4 until 32*nRC + nRAS - 1; truncate if necessary															
			32*nRC + nRAS	PRE	0	1	0	1	0	0	0	0	0	0	0	0	0	0	-
			…	Repeat pattern 1...4 until 32*nRC + nRC - 1; truncate if necessary															
		1	32*nRC + nRC + 0	ACT	0	0	0	1	1	0	1	1	0	0	0	0	0	0	-
			32*nRC + nRC + 1, 2	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			32*nRC + nRC + 3, 4	D_n, D_n	1	1	1	1	1	0	3	3	0	0	0	7	F	0	-
			…	Repeat pattern nRC + 1...4 until 32*nRC + 1 × nRC + nRAS - 1; truncate if necessary															
			32*nRC + 1 x nRC +nRCD - AL	RD	0	1	1	0	1	0	1	1	0	0	0	0	0	0	D0=96, D1=96 D2=96, D3=96 D4=96, D5=96 D6=96, D7=96
			…	Repeat pattern 1...4 until 32*nRC + nRAS - 1; truncate if necessary															
			32*nRC + 1 × nRC + nRAS	PRE	0	1	0	1	0	0	0	0	0	0	0	0	0	0	-
			…	Repeat pattern nRC + 1...4 until 2*nRC - 1; truncate if necessary															
		2	32*nRC + 2*nRC	repeat Sub-Loop 0, use BG[1:0] = 1, BA[1:0] = 2 instead															

		3	32*nRC + 3*nRC	repeat Sub-Loop 1, use BG[1:0] = 0, BA[1:0] = 3 instead
		4	32*nRC + 4*nRC	repeat Sub-Loop 0, use BG[1:0] = 1, BA[1:0] = 1 instead
		5	32*nRC + 5*nRC	repeat Sub-Loop 1, use BG[1:0] = 0, BA[1:0] = 2 instead
		6	32*nRC + 6*nRC	repeat Sub-Loop 0, use BG[1:0] = 1, BA[1:0] = 3 instead
		7	32*nRC + 7*nRC	repeat Sub-Loop 1, use BG[1:0] = 0, BA[1:0] = 0 instead
		8	32*nRC + 8*nRC	repeat Sub-Loop 1, use BG[1:0] = 2, BA[1:0] = 0 instead[1]
		9	32*nRC + 9*nRC	repeat Sub-Loop 0, use BG[1:0] = 3, BA[1:0] = 1 instead[1]
		10	32*nRC + 10*nRC	repeat Sub-Loop 1, use BG[1:0] = 2, BA[1:0] = 2 instead[1]
		11	32*nRC + 11*nRC	repeat Sub-Loop 0, use BG[1:0] = 3, BA[1:0] = 3 instead[1]
		12	32*nRC + 12*nRC	repeat Sub-Loop 1, use BG[1:0] = 2, BA[1:0] = 1 instead[1]
		13	32*nRC + 13*nRC	repeat Sub-Loop 0, use BG[1:0] = 3, BA[1:0] = 2 instead[1]
		14	32*nRC + 14*nRC	repeat Sub-Loop 1, use BG[1:0] = 2, BA[1:0] = 3 instead[1]
		15	32*nRC + 15*nRC	repeat Sub-Loop 0, use BG[1:0] = 3, BA[1:0] = 0 instead[1]

[1] For x8 devices only

Table 22 – IDD2N, IDD2NL, IDD2NG, IDD2ND, IDD2N_par, IPP2,IDD3N, and IDD3P Measurement-Loop Pattern[1]

CK_t /CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/	CAS_n/	WE_n/ A14	ODT	BG[1:0][2]	BA[1:0]	A12/BC_n	A[17,13,11	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[3]
Toggling	Static High	0	0	D, D	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
			1	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
			2	D_n, D_n	1	1	1	1	1	0	3	3	0	0	0	7	F	0	0
			3	D_n, D_n	1	1	1	1	1	1	3	3	0	0	0	7	F	0	0
		1	4-7	repeat Sub-Loop 0, use BG[1:0] = 1, BA[1:0] = 1 instead															
		2	8-11	repeat Sub-Loop 0, use BG[1:0] = 0, BA[1:0] = 2 instead															
		3	12-15	repeat Sub-Loop 1, use BG[1:0] = 1, BA[1:0] = 3 instead															
		4	16-19	repeat Sub-Loop 0, use BG[1:0] = 0, BA[1:0] = 1 instead															
		5	20-23	repeat Sub-Loop 1, use BG[1:0] = 1, BA[1:0] = 2 instead															
		6	24-27	repeat Sub-Loop 0, use BG[1:0] = 0, BA[1:0] = 3 instead															
		7	28-31	repeat Sub-Loop 1, use BG[1:0] = 1, BA[1:0] = 0 instead															
		8	32-35	repeat Sub-Loop 1, use BG[1:0] = 2, BA[1:0] = 0 instead															
		9	36-39	repeat Sub-Loop 0, use BG[1:0] = 3, BA[1:0] = 1 instead															
		10	40-43	repeat Sub-Loop 1, use BG[1:0] = 2, BA[1:0] = 2 instead															
		11	44-47	repeat Sub-Loop 0, use BG[1:0] = 3, BA[1:0] = 3 instead															
		12	48-51	repeat Sub-Loop 1, use BG[1:0] = 2, BA[1:0] = 1 instead															
		13	52-55	repeat Sub-Loop 0, use BG[1:0] = 3, BA[1:0] = 2 instead															
		14	56-59	repeat Sub-Loop 1, use BG[1:0] = 2, BA[1:0] = 3 instead															
		15	60-63	repeat Sub-Loop 0, use BG[1:0] = 3, BA[1:0] = 0 instead															

[1] DQS_t, DQS_c are VDDQ.
[2] BG1 is don't care for x16 device
[3] DQ signals are VDDQ

Table 23 – IDD2NT and IDDQ2NT Measurement-Loop Pattern[1]

CK_t /CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/	CAS_n/	WE_n/ A14	ODT	BG[1:0][2]	BA[1:0]	A12/BC_n	A[17,13,11	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[3]
Toggling	Static High	0	0	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
			1	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
			2	D_n, D_n	1	1	1	1	1	0	3	3	0	0	0	7	F	0	0
			3	D_n, D_n	1	1	1	1	1	0	3	3	0	0	0	7	F	0	0
		1	4-7	repeat Sub-Loop 0, use BG[1:0] = 1, BA[1:0] = 1 instead															
		2	8-11	repeat Sub-Loop 0, use BG[1:0] = 0, BA[1:0] = 2 instead															
		3	12-15	repeat Sub-Loop 1, use BG[1:0] = 1, BA[1:0] = 3 instead															
		4	16-19	repeat Sub-Loop 0, use BG[1:0] = 0, BA[1:0] = 1 instead															
		5	20-23	repeat Sub-Loop 1, use BG[1:0] = 1, BA[1:0] = 2 instead															
		6	24-27	repeat Sub-Loop 0, use BG[1:0] = 0, BA[1:0] = 3 instead															
		7	28-31	repeat Sub-Loop 1, use BG[1:0] = 1, BA[1:0] = 0 instead															
		8	32-35	repeat Sub-Loop 1, use BG[1:0] = 2, BA[1:0] = 0 instead															
		9	36-39	repeat Sub-Loop 0, use BG[1:0] = 3, BA[1:0] = 1 instead[4]															
		10	40-43	repeat Sub-Loop 1, use BG[1:0] = 2, BA[1:0] = 2 instead[4]															
		11	44-47	repeat Sub-Loop 0, use BG[1:0] = 3, BA[1:0] = 3 instead[4]															
		12	48-51	repeat Sub-Loop 1, use BG[1:0] = 2, BA[1:0] = 1 instead[4]															
		13	52-55	repeat Sub-Loop 0, use BG[1:0] = 3, BA[1:0] = 2 instead[4]															
		14	56-59	repeat Sub-Loop 1, use BG[1:0] = 2, BA[1:0] = 3 instead[4]															
		15	60-63	repeat Sub-Loop 0, use BG[1:0] = 3, BA[1:0] = 0 instead[4]															

[1] DQS_t, DQS_c are VDDQ.
[2] BG1 is don't care for x16 device
[3] DQ signals are VDDQ
[4] For x8 devices only

Table 24 – IDD4R, IDD4RB and IDDQ4R Measurement-Loop Pattern[1]

CK_t /CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/ A16	CAS_n/ A15	WE_n/ A14	ODT	BG[1:0][2]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[3]
Toggling	Static High	0	0	RD	0	1	1	0	1	0	0	0	0	0	0	0	0	0	D0=69,D1=69 D2=69,D3=69 D4=69,D5=69 D6=69,D7=69
			1	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			2,3	D_n, D_n	1	1	1	1	1	0	3	3	0	0	0	7	F	0	-
		1	4	RD	1	1	1	1	1	0	3	3	0	0	0	7	F	0	D0=96,D1=96 D2=96,D3=96 D4=96,D5=96 D6=96,D7=96
			5	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			6, 7	D_n, D_n	1	1	1	1	1	0	3	3	0	0	0	7	F	0	-
		2	8-11	repeat Sub-Loop 0, use BG[1:0] = 0, BA[1:0] = 2 instead															
		3	12-15	repeat Sub-Loop 1, use BG[1:0] = 1, BA[1:0] = 3 instead															
		4	16-19	repeat Sub-Loop 0, use BG[1:0] = 0, BA[1:0] = 1 instead															
		5	20-23	repeat Sub-Loop 1, use BG[1:0] = 1, BA[1:0] = 2 instead															
		6	24-27	repeat Sub-Loop 0, use BG[1:0] = 0, BA[1:0] = 3 instead															
		7	28-31	repeat Sub-Loop 1, use BG[1:0] = 1, BA[1:0] = 0 instead															
		8	32-35	repeat Sub-Loop 1, use BG[1:0] = 2, BA[1:0] = 0 instead[4]															
		9	36-39	repeat Sub-Loop 0, use BG[1:0] = 3, BA[1:0] = 1 instead[4]															
		10	40-43	repeat Sub-Loop 1, use BG[1:0] = 2, BA[1:0] = 2 instead[4]															
		11	44-47	repeat Sub-Loop 0, use BG[1:0] = 3, BA[1:0] = 3 instead[4]															
		12	48-51	repeat Sub-Loop 1, use BG[1:0] = 2, BA[1:0] = 1 instead[4]															
		13	52-55	repeat Sub-Loop 0, use BG[1:0] = 3, BA[1:0] = 2 instead[4]															
		14	56-59	repeat Sub-Loop 1, use BG[1:0] = 2, BA[1:0] = 3 instead[4]															
		15	60-63	repeat Sub-Loop 0, use BG[1:0] = 3, BA[1:0] = 0 instead[4]															

[1] DQS_t, DQS_c are used according to RD Commands, otherwise VDDQ.
[2] BG1 is don't care for x16 device
[3] Burst Sequence driven on each DQ signal by Read Command.
[4] For x8 devices only

Table 25 – IDD4W, IDD4WB and IDD4W_par Measurement-Loop Pattern[1]

CK_t /CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/ A16	CAS_n/ A15	WE_n/ A14	ODT	BG[1:0][2]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[3]
Toggling	Static High	0	0	WR	0	1	1	0	1	0	0	0	0	0	0	0	0	0	D0=69,D1=69 D2=69,D3=69 D4=69,D5=69 D6=69,D7=69
			1	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			2,3	D_n, D_n	1	1	1	1	1	0	3	3	0	0	0	7	F	0	-
		1	4	WR	0	1	1	0	1	0	1	1	0	0	0	7	F	0	D0=96,D1=96 D2=96,D3=96 D4=96,D5=96 D6=96,D7=96
			5	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			6, 7	D_n, D_n	1	1	1	1	1	0	3	3	0	0	0	7	F	0	-
		2	8-11	repeat Sub-Loop 0, use BG[1:0] = 0, BA[1:0] = 2 instead															
		3	12-15	repeat Sub-Loop 1, use BG[1:0] = 1, BA[1:0] = 3 instead															
		4	16-19	repeat Sub-Loop 0, use BG[1:0] = 0, BA[1:0] = 1 instead															
		5	20-23	repeat Sub-Loop 1, use BG[1:0] = 1, BA[1:0] = 2 instead															
		6	24-27	repeat Sub-Loop 0, use BG[1:0] = 0, BA[1:0] = 3 instead															
		7	28-31	repeat Sub-Loop 1, use BG[1:0] = 1, BA[1:0] = 0 instead															
		8	32-35	repeat Sub-Loop 1, use BG[1:0] = 2, BA[1:0] = 0 instead[4]															
		9	36-39	repeat Sub-Loop 0, use BG[1:0] = 3, BA[1:0] = 1 instead[4]															
		10	40-43	repeat Sub-Loop 1, use BG[1:0] = 2, BA[1:0] = 2 instead[4]															
		11	44-47	repeat Sub-Loop 0, use BG[1:0] = 3, BA[1:0] = 3 instead[4]															
		12	48-51	repeat Sub-Loop 1, use BG[1:0] = 2, BA[1:0] = 1 instead[4]															
		13	52-55	repeat Sub-Loop 0, use BG[1:0] = 3, BA[1:0] = 2 instead[4]															
		14	56-59	repeat Sub-Loop 1, use BG[1:0] = 2, BA[1:0] = 3 instead[4]															
		15	60-63	repeat Sub-Loop 0, use BG[1:0] = 3, BA[1:0] = 0 instead[4]															

[1] DQS_t, DQS_c are used according to WR Commands, otherwise VDDQ..
[2] BG1 is don't care for x16 device
[3] Burst Sequence driven on each DQ signal by Write Command.
[4] For x8 devices only

Table 26 – IDD5B Measurement-Loop Pattern[1]

CK_t /CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/ A16	CAS_n/ A15	WE_n/ A14	ODT	BG[1:0][2]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[3]
Toggling	Static High	0	0	REF	0	1	1	0	1	0	0	0	0	0	0	0	0	0	-
		1	1	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			2	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			3	D_n, D_n	0	1	1	0	1	0	1	1	0	0	0	7	F	0	-
			4	D_n, D_n	1	1	1	1	1	0	3	3	0	0	0	7	F	0	-
			5-7	repeat pattern 1...4, use BG[1:0] = 1, BA[1:0] = 1 instead															
			8-11	repeat pattern 1...4, use BG[1:0] = 0, BA[1:0] = 2 instead															
			12-15	repeat pattern 1...4, use BG[1:0] = 1, BA[1:0] = 3 instead															
			16-19	repeat pattern 1...4, use BG[1:0] = 0, BA[1:0] = 1 instead															
			20-23	repeat pattern 1...4, use BG[1:0] = 1, BA[1:0] = 2 instead															
			24-27	repeat pattern 1...4, use BG[1:0] = 0, BA[1:0] = 3 instead															
			28-31	repeat pattern 1...4, use BG[1:0] = 1, BA[1:0] = 0 instead															
			32-35	repeat pattern 1...4, use BG[1:0] = 2, BA[1:0] = 0 instead[4]															
			36-39	repeat pattern 1...4, use BG[1:0] = 3, BA[1:0] = 1 instead[4]															
			40-43	repeat pattern 1...4, use BG[1:0] = 2, BA[1:0] = 2 instead[4]															
			44-47	repeat pattern 1...4, use BG[1:0] = 3, BA[1:0] = 3 instead[4]															
			48-51	repeat pattern 1...4, use BG[1:0] = 2, BA[1:0] = 1 instead[4]															
			52-55	repeat pattern 1...4, use BG[1:0] = 3, BA[1:0] = 2 instead[4]															
			56-59	repeat pattern 1...4, use BG[1:0] = 2, BA[1:0] = 3 instead[4]															
			60-63	repeat pattern 1...4, use BG[1:0] = 3, BA[1:0] = 0 instead[4]															
		2	64 ... nRFC - 1	repeat Sub-Loop 1, Truncate, if necessary															

[1] DQS_t, DQS_c are VDDQ
[2] BG1 is don't care for x16 device
[3] DQ signals are VDDQ
[4] For x8 devices only

Table 27 – IDD7 Measurement-Loop Pattern[1,2]

CK_t /CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/ A16	CAS_n/ A15	WE_n/ A14	ODT	[1:0][3]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
Toggling	Static High	1A	0	ACT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
			1,2	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	
			3,4	D_n, D_n	1	1	1	1	1	0	3	3	0	0	0	7	F	0	
			…	repeat pattern 1...4 until nRCD - 1, truncate if necessary															
			nRCD	WR	0	1	1	0	0	1	0	0	0	0	0	0	0	0	D0=69,D1=69 D2=69,D3=69 D4=69,D5=69 D6=69,D7=69
			…	repeat pattern 1...4 until nRC - nRP - 1, truncate if necessary															
			nRC-nRP	PRE	0	1	0	1	0	0	0	0	0	0	0	0	0	0	
			…	repeat pattern 1...4 until nRC-1, truncate if necessary															
		2A	nRC	ACT	0	0	0	0	0	0	0	0	0	0	7	F	0	0	
			nRC + 1, 2	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	
			nRC + 3, 4	D_n, D_n	1	1	1	1	1	0	3	0	0	0	7	F	0	0	
			…	repeat pattern nRC+1...4 until nRC + nRCD - 1, truncate if necessary															
			nRC + nRCD	WR	0	1	1	0	0	1	0	0	0	0	0	0	0	0	D0=96,D1=96 D2=96,D3=96 D4=96,D5=96 D6=96,D7=96
			…	repeat cycles 1...4 until nRC+(nRC-nRP)- 1, truncate if necessary															
			nRC+(nRC-nRP)	PRE	0	1	0	1	0	0	0	0	0	0	0	0	0	0	
			…	repeat pattern 1...4 until 2*nRC - 1, truncate if necessary															
		3A	2*nRC	Repeat subloop 1A, use BG[1:0]=1, use BA[1:0]=1 instead (bank 5)															
			3*nRC	Repeat subloop 2A, use BG[1:0]=1, use BA[1:0]=1 instead (bank 5)															
			4*nRC	Repeat subloop 1A, use BG[1:0]=0, use BA[1:0]=2 instead (bank 2)															
			5*nRC	Repeat subloop 2A, use BG[1:0]=0, use BA[1:0]=2 instead (bank 2)															
			6*nRC	Repeat subloop 1A, use BG[1:0]=1, use BA[1:0]=3 instead (bank 7)															
			7*nRC	Repeat subloop 2A, use BG[1:0]=1, use BA[1:0]=3 instead (bank 7)															
			8*nRC	Repeat subloop 1A, use BG[1:0]=0, use BA[1:0]=1 instead (bank 1)															
			9*nRC	Repeat subloop 2A, use BG[1:0]=0, use BA[1:0]=1 instead (bank 1)															

[1] DQS_t, DQS_c are VDDQ

[2] Before running this test make sure the two write procedure has been correctly implemented. See "**Error! Reference source not found.**". Each test loop is required to alternate between two addresses, A[15:00]=0x0000 and A[15:00]=0x03F8 during ACT to ensure accurate current measurements.

[3] BG1 is don't care for x16 device

[4] Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are VDDQ.

CK_t /CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/ A16	CAS_n/ A15	WE_n/ A14	ODT	[1:0][3]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
			10*nRC	Repeat subloop 1A, use BG[1:0]=1, use BA[1:0]=2 instead (bank 6)															
			11*nRC	Repeat subloop 2A, use BG[1:0]=1, use BA[1:0]=2 instead (bank 6)															
			12*nRC	Repeat subloop 1A, use BG[1:0]=0, use BA[1:0]=3 instead (bank 3)															
			13*nRC	Repeat subloop 2A, use BG[1:0]=0, use BA[1:0]=3 instead (bank 3)															
			14*nRC	Repeat subloop 1A, use BG[1:0]=1, use BA[1:0]=0 instead (bank 4)															
			15*nRC	Repeat subloop 2A, use BG[1:0]=1, use BA[1:0]=0 instead (bank 4)															
			16*nRC	Repeat subloop 1A, use BG[1:0]=2, use BA[1:0]=0 instead (bank 8)[1]															
			17*nRC	Repeat subloop 2A, use BG[1:0]=2, use BA[1:0]=0 instead (bank 8)[1]															
			18*nRC	Repeat subloop 1A, use BG[1:0]=3, use BA[1:0]=1 instead (bank 13)[1]															
			19*nRC	Repeat subloop 2A, use BG[1:0]=3, use BA[1:0]=1 instead (bank 13)[1]															
			20*nRC	Repeat subloop 1A, use BG[1:0]=2, use BA[1:0]=2 instead (bank 10)[1]															
			21*nRC	Repeat subloop 2A, use BG[1:0]=2, use BA[1:0]=2 instead (bank 10)[1]															
			22*nRC	Repeat subloop 1A, use BG[1:0]=3, use BA[1:0]=3 instead (bank 15)[1]															
			23*nRC	Repeat subloop 2A, use BG[1:0]=3, use BA[1:0]=3 instead (bank 15)[1]															
			24*nRC	Repeat subloop 1A, use BG[1:0]=2, use BA[1:0]=1 instead (bank 9)[1]															
			25*nRC	Repeat subloop 2A, use BG[1:0]=2, use BA[1:0]=1 instead (bank 9)[1]															
			26*nRC	Repeat subloop 1A, use BG[1:0]=3, use BA[1:0]=2 instead (bank 14)[1]															
			27*nRC	Repeat subloop 2A, use BG[1:0]=3, use BA[1:0]=2 instead (bank 14)[1]															
			28*nRC	Repeat subloop 1A, use BG[1:0]=2, use BA[1:0]=3 instead (bank 11)[1]															
			29*nRC	Repeat subloop 2A, use BG[1:0]=2, use BA[1:0]=3 instead (bank 11)[1]															
			30*nRC	Repeat subloop 1A, use BG[1:0]=3, use BA[1:0]=0 instead (bank 12)[1]															
			31*nRC	Repeat subloop 2A, use BG[1:0]=3, use BA[1:0]=0 instead (bank 12)[1]															
		1	32*nRC	ACT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			32*nRC + 1	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			32*nRC + 2	D_n	1	1	1	1	1	0	3	3	0	0	0	7	F	0	-
			32*nRC + 3	Repeat last 2 cycles until (32*nRC) + nRRD - 1, truncate if necessary															
		2	32*nRC + nRRD	Repeat loop 1, use BG[1:0]=1,BA[1,0]=1 (bank 5) instead															
			32*nRC + 2*nRRD	Repeat loop 1, use BG[1:0]=0,BA[1,0]=2 (bank 2) instead															
			32*nRC + 3*nRRD	Repeat loop 1, use BG[1:0]=1,BA[1,0]=3 (bank 7) instead															
		3	32*nRC + 4*nRRD	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			32*nRC + 4*nRRD+1	D_n	1	1	1	1	1	0	3	3	0	0	0	7	F	0	-
			…	Repeat the above 2 cycles until (32*nRC) + nRCD - 1															
		4	32*nRC + nRCD	RDA	0	1	1	0	1	0	0	0	0	0	1	0	0	0	D0=69,D1=69 D2=69,D3=69 D4=69,D5=69

[1] For x8 devices only

CK_t /CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/ A16	CAS_n/ A15	WE_n/ A14	ODT	[1:0][3]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
																			D6=69,D7=69
			32*nRC + nRCD+1	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			32*nRC + nRCD+2	D_n	1	1	1	1	1	0	3	3	0	0	0	7	F	0	-
			…	Repeat last two cycles until (32*nRC) + nRCD+ nRRD-1															
		5	32*nRC + nRCD + nRRD	Repeat loop 4, use BG[1:0]=1,BA[1,0]=1 (bank 5) instead															
			32*nRC + nRCD + 2*nRRD	Repeat loop 4, use BG[1:0]=0,BA[1,0]=2 (bank 2) instead															
			32*nRC + nRCD + 3*nRRD	Repeat loop 4, use BG[1:0]=1,BA[1,0]=3 (bank 7) instead															
		6	32*nRC + nRCD + 4*nRRD	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			32*nRC + nRCD + 4*nRRD+1	D_n	1	1	1	1	1	0	3	3	0	0	0	7	F	0	-
			…	Repeat last two cycles until (32*nRC) + nFAW - 1															
		7	32*nRC + nFAW	Repeat Sub-Loop 1, use BG[1:0] = 0, BA[1:0] = 1 instead (Bank 1)															
			32*nRC + nFAW + nRRD	Repeat Sub-Loop 1, use BG[1:0] = 1, BA[1:0] = 2 instead (Bank 6)															
			32*nRC + nFAW + 2*nRRD	Repeat Sub-Loop 1, use BG[1:0] = 0, BA[1:0] = 3 instead (Bank 3)															
			32*nRC + nFAW + 3*nRRD	Repeat Sub-Loop 1, use BG[1:0] = 1, BA[1:0] = 0 instead (Bank 4)															
			32*nRC + nFAW + 4*nRRD	Repeat Sub-Loop 3 until 32*nRC+nFAW+nRCD-1															
			32*nRC + nFAW+nRCD	Repeat subloop 4, use BG[1:0]=0, BA[1:0]=1 instead (Bank 1)															
			32*nRC + nFAW+nRCD + nRRD	Repeat subloop 4, use BG[1:0]=1, BA[1:0]=2 instead (Bank 6)															
			32*nRC + nFAW+nRCD + 2*nRRD	Repeat subloop 4, use BG[1:0]=0, BA[1:0]=3 instead (Bank 3)															
			32*nRC + nFAW+nRCD + 3*nRRD	Repeat subloop 4, use BG[1:0]=1, BA[1:0]=0 instead (Bank 4)															
			32*nRC + nFAW+nRCD + 4*nRRD	Repeat Sub-Loop 3 until 32*nRC+2*nFAW-1															

CK_t /CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/ A16	CAS_n/ A15	WE_n/ A14	ODT	[1:0][3]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
		8	32*nRC + 2*nFAW	Repeat Sub-Loop 1, use BG[1:0] = 2, BA[1:0] = 0 instead (Bank 8)[1]															
			32*nRC + 2*nFAW+ nRRD	Repeat Sub-Loop 1, use BG[1:0] = 3, BA[1:0] = 1 instead (Bank 13)[1]															
			32*nRC + 2*nFAW + 2*nRRD	Repeat Sub-Loop 1, use BG[1:0] = 2, BA[1:0] = 2 instead (Bank 10)[1]															
			32*nRC + 2*nFAW + 3*nRRD	Repeat Sub-Loop 1, use BG[1:0] = 3, BA[1:0] = 3 instead (Bank 15)[1]															
			32*nRC + 2*nFAW + 4*nRRD	Repeat Sub-Loop 3 until 32*nRC+2*nFAW+nRCD-1															
			32*nRC + 2*nFAW+nRCD	Repeat subloop 4, use BG[1:0]=2, BA[1:0]=0 instead (Bank 8)[1]															
			32*nRC + 2*nFAW+nRCD + nRRD	Repeat subloop 4, use BG[1:0]=3, BA[1:0]=1 instead (Bank 13)[1]															
			32*nRC + 2*nFAW+nRCD + 2*nRRD	Repeat subloop 4, use BG[1:0]=2, BA[1:0]=2 instead (Bank 10)[1]															
			32*nRC + 2*nFAW+nRCD + 3*nRRD	Repeat subloop 4, use BG[1:0]=3, BA[1:0]=3 instead (Bank 15)[1]															
			32*nRC + 2*nFAW+nRCD + 4*nRRD	Repeat Sub-Loop 3 until 32*nRC+3*nFAW-1															
		9	32*nRC + 3*nFAW	Repeat Sub-Loop 1, use BG[1:0] = 2, BA[1:0] = 1 instead (Bank 9)[1]															
			32*nRC + 3*nFAW+ nRRD	Repeat Sub-Loop 1, use BG[1:0] = 3, BA[1:0] = 2 instead (Bank 14)[1]															
			32*nRC + 3*nFAW + 2*nRRD	Repeat Sub-Loop 1, use BG[1:0] = 2, BA[1:0] = 3 instead (Bank 11)[1]															
			32*nRC + 3*nFAW + 3*nRRD	Repeat Sub-Loop 1, use BG[1:0] = 3, BA[1:0] = 0 instead (Bank 12)[1]															
			32*nRC + 3*nFAW + 4*nRRD	Repeat Sub-Loop 3 until 32*nRC+3*nFAW+nRCD-1															
			32*nRC+ 3*nFAW+nRCD	Repeat subloop 4, use BG[1:0]=2, BA[1:0]=1 instead (Bank 9)[1]															
			32*nRC+ 3*nFAW+nRCD+ nRRD	Repeat subloop 4, use BG[1:0]=3, BA[1:0]=2 instead (Bank 14)[1]															
			32*nRC+ 3*nFAW+nRCD+ 2*nRRD	Repeat subloop 4, use BG[1:0]=2, BA[1:0]=3 instead (Bank 11)[1]															

[1] For x8 devices only

CK_t /CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/ A16	CAS_n/ A15	WE_n/ A14	ODT	[1:0][3]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
			32*nRC+ 3*nFAW+nRCD+ 3*nRRD	Repeat subloop 4, use BG[1:0]=3, BA[1:0]=0 instead (Bank 12)[1]															
			32*nRC+ 3*nFAW+nRCD+ 4*nRRD	Repeat Sub-Loop1 until 32*nRC+4*nFAW-1															
		10	32*nRC + 4*nFAW	Repeat Sub-loop 3 until nRC - 1, if nRC > 4*nFAW. Truncate if necessary															

9. ELECTRICAL CHARACTERISTICS AND AC TIMING PARAMETERS

Electrical Characteristics and AC Timing parameters are as follows.

Table 28 – Clock Timing

Parameter		Symbol	ST-DDR4-1333		Units
			Min	Max	
Clock Period Average (DLL off mode)		tCK (DLL_OFF)	8	-	ns
Clock Period Average[1]		tCK (DLL_OFF)	8	-	ns
High pulse width average		tCH (AVG)	0.48	0.52	CK
Low pulse width average		tCL (AVG)	0.48	0.52	CK
Clock period jitter	Total	tJITper_tot	-63	63	ps
	Deterministic	tJITper_dj	-31	31	ps
	DLL Locking	tJITper,lck	-50	50	ps
Clock absolute period		tCK (ABS	MIN = tCK (AVG) MIN + tJITper_tot MIN; MAX = tCK(AVG) MAX + tJITper_tot MAX		ps
Clock absolute high pulse width (includes duty cycle jitter) (includes duty cycle jitter)		tCH (ABS)	0.45	-	tCK (AVG)
Clock absolute low pulse width (includes duty cycle jitter)		tCL (ABS)	0.45	-	tCK (AVG)

[1] Applicable from tCK (AVG) MIN to tCK (AVG) MAX as stated in the Speed Bin tables.

Parameter		Symbol	ST-DDR4-1333		Units
			Min	Max	
Cycle-to-cycle jitter	Total	tJITper_tot	125		ps
	Deterministic	tJITper_dj	3		
	DLL Locking	tJITper,lck	100		
Cumulative Error across	2 cycles	tERR2per	-92	92	ps
	3 cycles	tERR3per	-109	109	ps
	4 cycles	tERR4per	-121	121	ps
	5 cycles	tERR5per	-131	131	ps
	6 cycles	tERR6per	-139	139	ps
	7 cycles	tERR7per	-145	145	ps
	8 cycles	tERR8per	-151	151	ps
	9 cycles	tERR9per	-156	156	ps
	10 cycles	tERR10per	-160	160	ps
	11 cycles	tERR11per	-164	164	ps
	12 cycles	tERR12per	-168	168	ps
	n = 13, 14, … 49, 50 cycles	tERRnper	tERRnper MIN = (1 + 0.68ln[n]) × tJITper MIN tERRnper MAX = (1 + 0.68ln[n]) × tJITper MAX 145-124124-109109		ps

Table 29 – DQ Input Timing

Parameter		Symbol	DDR4-133		Units
			Min	Max	
Data setup time to DQS_t, DQS_c	Base (calibrated Vref)	tDS	Refer to DQ Input Receiver Specification section (approximately 0.15tCK to 0.35tCK		-
	Non-calibrated Vref	tPDA_S	minimum of 0.5ui		ui
Data hold time from DQS_t, DQS_c	Base (calibrated Vref)	tDH	Refer to DQ Input Receiver Specification section (approximately 0.15tCK to 0.35tCK		
	Non-calibrated Vref	tPDA_H	minimum of 0.5ui		ui

DQ and DM minimum data pulse width for each input	tDIPW	0.58	-	UId

Table 30 – DQ Output Timing

Parameter	Symbol	DDR4-133		Units
		Min	Max	
DQS_t, DQS_c to DQ skew, per group, per access	tDQSQ	-	0.16	UId
DQ output hold time from DQS_t, DQS_c	tQH	0.76	-	UId
Data valid window per device: tQH - DQSQ for a device	tDVWd	0.63	-	UId
Data valid window per device per pin: tQH - tDQSQ per pin for a device	tDVWp	0.66	-	UId
DQ Low-Z time from CK_t, CK_c	tLZDQ	-450	225	ps
DQ High-Z time from CK_t, CK_c	tHZDQ	-	225	ps

Table 31 – DQ Strobe Input Timing

Parameter	Symbol	ST-DDR4-1333		Units
		Min	Max	
DQS_t, DQS_c rising edge to CK_t, CK_c rising edge	tDQSS	-0.27	0.27	CK
DQS_t, DQS_c differential input low pulse width	tDQSL	0.46	0.54	CK
DQS_t, DQS_c differential input high pulse width	tDQSH	0.46	0.54	CK
DQS_t, DQS_c falling edge setup to CK_t, CK_c rising edge	tDSS	0.18	-	CK
DQS_t, DQS_c falling edge hold from CK_t, CK_c rising edge	tDSH	0.18	-	CK
DQS_t, DQS_c differential WRITE preamble	tWPRE	0.9	-	CK
DQS_t, DQS_c differential WRITE postamble	tWPST	0.33	-	CK

Table 32 – DQ Strobe Output Timing

Parameter	Symbol	ST-DDR4-1333		Units
		Min	Max	
DQS_t, DQS_c rising edge output access time from rising CK_t, CK_c	tDQSCK	-225	225	ps
DQS_t, DQS_c rising edge output variance window per MRAM	tDQSCKi	-	370	ps
DQS_t, DQS_c differential output high time	tQSH	0.38	-	CK
DQS_t, DQS_c differential output low time	tQSL	0.38	-	CK
DQS_t, DQS_c Low-Z time (RL - 1)	tLZDQS	-450	225	ps
DQS_t, DQS_c High-Z time (RL + BL/2)	tHZDQS	-	225	ps
DQS_t, DQS_c differential READ preamble	tRPRE	0.9	-	CK
DQS_t, DQS_c differential READ postamble	tRPST	0.33	-	CK

Table 33 – Command and Address Timing

Parameter		Symbol	ST-DDR4-1333		Units
			Min	Max	
DLL Locking Time		tDLLK	597	-	CK
CMD, ADDR setup time to CK_t, CK_c referenced to VIH(AC) and VIL(AC) levels	Base	tIS	115	-	ps
	VREFCA	tISVREF	215	-	ps
CMD, ADDR hold time to CK_t, CK_c referenced to VIH(DC) and VIL(DC) levels	Base	tIH	140	-	ps
	VREFCA	tIHVREF	215	-	ps
CTRL, ADDR pulse width for each input		tIPW	600	-	ps
ACTIVATE to internal READ or WRITE delay		tRCD[1]	135	-	ns
PRECHARGE command period		tRP[1]	7.5	-	ns
STORE operation period		tST[2]	380	-	ns
ACTIVATE-to-PRECHARGE command period		tRAS[1]	143	-	ns
ACTIVATE-to-ACTIVATE or REF command period		tRC[1]	190	-	ns
ACTIVATE-to-ACTIVATE command period to different bank groups		tRRD_S	10	-	ns
ACTIVATE-to-ACTIVATE command period to same bank group		tRRD_L	10	-	ns
Four ACTIVATE windows		tFAW	240	-	ns

[1] See “Table 2 - JESD79-4A Specification Deviations” and “Table 18 – ST-DDR4-1333 Speed Bin Operating Conditions”

[2] See “Table 1 - JESD79-4A Specification Enhancements and “Table 18 – ST-DDR4-1333 Speed Bin Operating Conditions”

Table 34 – Command and Address Timing with (CL)

Parameter	Symbol	CL	ST-DDR4-1333		Units
			Min	Max	
WRITE recovery time	tWR	-	15	-	ns
Delay from start of internal WRITE transaction to internal READ command – Both same bank group and different bank group for BL8	tWTR_L and tWTR_S	10	4	-	CK
Delay from start of internal WRITE transaction to internal READ command – Both same bank group and different bank group for BC4	tWTR_L and tWTR_S	10	6	-	CK
READ-to-PRECHARGE time	tRTP	MIN = greater of 4CK or 7.5ns			CK
CAS_n-to-CAS_n command delay to different bank group	tCCD_S		4	-	CK
CAS_n-to-CAS_n command delay to same bank group	tCCD_S		4	-	CK
Auto precharge write recovery + precharge time	tDAL	MIN = WR + ROUNDUP(tRP/tCK(AVG)); MAX = N/A			CK

Table 35 – MRS Command Timing

Parameter	Symbol	ST-DDR4-1333		Units
		Min	Max	
MRS command cycle time	tMRD	8	-	CK
MRS command cycle time in PDA mode	tMRD_PDA	MIN = greater of (16nCK, 10ns)		CK
MRS command update delay	tMOD	MIN = 24		CK
MRS command update delay in PDA mode	tMOD_PDA	MIN = tMOD		CK
MRS command to DQS drive in preamble training	tSDO	MIN = tMOD + 9ns		ns

Table 36 – MPR Command Timing

Parameter	Symbol	ST-DDR4-1333		Units
		Min	Max	
Multipurpose register recovery time	tMPRR	MIN = 1		CK
Multipurpose register write recovery time	tWR_MPR	MIN = tMOD		CK

Table 37 – Connectivity Test Timing

Parameter	Symbol	ST-DDR4-1333		Units
		Min	Max	
TEN pin HIGH to CS_n LOW – Enter CT mode	tCT_Enable	200	-	ns
CS_n LOW and valid input to valid output	tCT_Valid	-	200	ns
CK_t, CK_c valid and CKE HIGH after TEN goes HIGH	tCTECT_Valid[1]	10	-	ns

Table 38 – Calibration and V_{REFDQ} Train Timing

Parameter	Symbol	ST-DDR4-1333		Units
		Min	Max	
ZQCL command: Long calibration time	tZQinit	1024	-	ns
	tZQoper	512	-	ns
The V_{REF} increment/decrement step time	VREF_time	MIN = 150		ns
Enter V_{REFDQ} training mode to the first write or V_{REFDQ} MRS command delay	tVREFDQE	MIN=150		ns
Exit V_{REFDQ} training mode to the first WRITE command delay	tVREFDQX	MIN=150		ns

[1] CK_t and CK-c must be complementary during Connectivity Test maintaining differential input

Table 39 – Initialization and Reset Timing

Parameter	Symbol	ST-DDR4-1333		Units
		Min	Max	
Exit reset from CKE HIGH to a valid command	tXPR	MIN = greater of 5CK or tRFC (MIN) + 10ns		ns
RESET_L pulse low after power stable	tPW_RESET_S	20	-	µs
RESET_L pulse low at power-up	tPW_RESET_L	200	-	µs
Begin power supply ramp to power supplies stable	tVDDPR	N/A	200	ms
RESET_n LOW to power supplies stable	tRPS	0	0	ns
RESET_n LOW to I/O and R_{TT} High-Z	tIOZ	N/A	undefined	ns

Table 40 – Refresh Timing

Parameter	Symbol	ST-DDR4-1333		Units
		Min	Max	
REFRESH-to-ACTIVATE or REFRESH command period (all bank groups)[1]	tRFC	tRFC= tST[2]		ns
Average periodic refresh interval	tREFI	See Note 3[3]		µs

Table 41 – Self-Refresh Timing

Parameter	Symbol	ST-DDR4-1333		Units
		Min	Max	
Exit self-refresh to commands not requiring a locked DLL SRX to commands not requiring a locked DLL in self-refresh abort[4]	tXS	10	-	ns
Exit self-refresh to ZQCL, and MRS (CL, CWL, WR, RTP and geardown)[4]	tXS_FAST	10	-	ns
Exit self-refresh to commands requiring a locked DLL	tXSDLL	tDLLK (MIN)	-	CK

[1] The ST-DDR4 device does not support the Fine Granularity Refresh Mode. These parameters are referenced to tRFC.
[2] tST is specified in Table 18 – ST-DDR4-1333 Speed Bin Operating Conditions and Table 65 – Bank Staggering Time
[3] A refresh interval is not required. However, a REFRESH command may be used to ensure last data written is persistent.
[4] The ST-DDR4 device does not support Fine Granularity Refresh Mode. These parameters are referenced to tRFC.

Parameter	Symbol	ST-DDR4-1333		Units
		Min	Max	
Minimum CKE low pulse width for self-refresh entry to self-refresh exit timing	tCKESR	tST[1]	-	CK
Valid clocks after self-refresh entry (SRE) or power-down entry (PDE)	tCKSRE	MAX (5CK,10ns)	-	CK
Valid clocks before self-refresh exit (SRX) or power-down exit (PDX), or reset exit	tCKSRX	MAX (5CK,10ns)	-	CK

Table 42 – Power Down Timing

Parameter	Symbol	ST-DDR4-1333		Units
		Min	Max	
Exit power-down with DLL on to any valid command	tXP	MAX (4CK,6ns)	-	CK
CKE MIN pulse width	tCKE(MIN)	MAX (3CK,5ns)	-	CK
Command pass disable delay	tCPDED	8	-	CK
Power-down entry to power-down exit timing	tPD	tCKE (MIN)	-	CK
Begin power-down period prior to CKE registered HIGH	tANPD	WL - 1CK	WL - 1CK	CK
Power-down entry period: ODT either synchronous or asynchronous	PDE	Greater of tANPD or tRFC REFRESH command to CKE LOW time		CK
Power-down exit period: ODT either synchronous or asynchronous	PDX	tANPD + tXPDLL		CK
ACTIVATE command to power-down entry	tACTPDEN	1		CK
PRECHARGE/PRECHARGE ALL command to power-down entry	tPRPDEN	1	-	CK
REFRESH command to power-down entry	tREFPDEN	1	-	CK
MRS command to power-down entry	tMRSPDEN	tMOD (MIN)	-	CK
READ/READ with auto precharge command to power-down entry	tRDPDEN	MIN = RL + 4 + 1		CK
WRITE command to power-down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	MIN = WL + 4 + tWR / tCK(AVG)		CK
WRITE command to power-down entry (BC4MRS)	tWRPBC4DEN	MIN = WL + 2 + tWR / tCK(AVG)		CK

[1] tST is specified in Table 18 – ST-DDR4-1333 Speed Bin Operating Conditions and Table 65 – Bank Staggering Time.

Parameter	Symbol	ST-DDR4-1333		Units
		Min	Max	
WRITE with auto precharge command to power-down entry (BL8OTF, BL8MRS,BC4OTF)	tWRAPDEN	MIN = WL + 4 + WR + 1		CK
WRITE with auto precharge command to power-down entry (BC4MRS)	tWRAPBC4DEN	MIN = WL + 2 + WR + 1		CK

Table 43 – Write Leveling Timing

Parameter	Symbol	ST-DDR4-1333		Units
		Min	Max	
First DQS_t, DQS_c rising edge after write leveling mode is programmed	tWLMRD	40	-	CK
DQS_t, DQS_c delay after write leveling mode is programmed	tWLDQSEN	25	-	CK
Write leveling setup from rising CK_t, CK_cr crossing to rising DQS_t, DQS_c crossing	tWLS	0.13	-	CK
Write leveling hold from rising DQS_t, DQS_c crossing to rising CK_t, CK_c crossing	tWLH	0.13	-	CK
Write leveling output delay	tWLO	0	9.5	ns
Write leveling output error	tWLOE	0	2	ns

10. POWER UP INITIALIZATION SEQUENCE

10.1 Default Values

For power-up and reset initialization, in order to prevent the device from functioning improperly default values for the following MR settings need to be defined.

- Gear down mode MR3 A[3]): 0 = 1/2 Rate
- Per device Addressability (PDA) (MR3 A[4]): 0 = Disable
- Max Power Saving Mode (MR4 A[1]): 0 = Disable
- CS to Command/Address Latency (MR4 A[8:6]): 000 = Disable
- CA Parity Latency Mode (MR5 A[2:0]): 000 = Disable

10.2 Power Up Initialization Sequence

1. Apply power (RESET_n is recommended to be maintained below 0.2 x V_{DD}; all other inputs may be undefined). RESET_n needs to be maintained for minimum 200µs with stable power. CKE is pulled “L” any time before RESET_n being de-asserted (minimum time 10ns). The power voltage ramp time between 300mV to $V_{DD\ min}$ must be no greater than 200ms; and

during the ramp, $V_{DD} \geq V_{DDQ}$ and (V_{DD}- V_{DDQ}) < 0.3V. VPP must ramp at the same time or earlier than VDD and VPP must be equal to or higher than VDD at all times.

During power up, either of the following conditions may exist and must be met:

- Apply V_{PP} without any slope reversal before or at the same time as V_{DD} and V_{DDQ}.
- V_{DD} and V_{DDQ} are driven from a single power converter output and apply V_{DD}/V_{DDQ} without any slope reversal before or at the same time as V_{TT} and V_{REFCA}.
- The voltage levels on all pins other than V_{DD}, V_{DDQ}, V_{SS}, V_{SSQ} must be less than or equal to V_{DDQ} and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side.
- V_{TT} is limited to 0.76V max once power ramp is finished.
- VREFCA tracks VDD/2.

or

- Apply V_{PP} without any slope reversal before or at the same time as V_{DD}.
- Apply VDD without any slope reversal before or at the same time as VDDQ.
- Apply V_{DDQ} without any slope reversal before or at the same time as V_{TT} & V_{REFCA}.
- The voltage levels on all pins other than V_{PP}, V_{DD}, V_{DDQ}, V_{SS}, V_{SSQ} must be less than or equal to

V_{DDQ} and V_{DD} on one side and must be larger than or equal to V_{SSQ} and V_{SS} on the other side.

2. After RESET_n is de-asserted, wait for another 500µs until CKE becomes active. During this time, the device will start internal initialization; this will be done independently of external clocks.
3. Clocks (CK_t, CK_c) need to be started and stabilized for at least 10ns or 5tCK (whichever is larger) before CKE goes active. Since CKE is a synchronous signal, the corresponding setup time to clock (tIS) must be met. Also a DESELECT command must be registered (with tIS set up time to clock) at clock edge Td. Once the CKE is registered “High” after Reset, CKE needs to be continuously registered “High” until the initialization sequence is finished, including expiration of tDLLK and tZQinit.
4. The ST-DDR4 device keeps its on-die termination in high-impedance state as long as RESET_n is asserted. Further, the device keeps its on-die termination in the high impedance state after RESET_n deassertion until CKE is registered HIGH. The ODT input signal may be in undefined state until tIS before CKE is registered HIGH. When CKE is registered HIGH, the ODT input signal may be statically held at either LOW or HIGH. If $R_{TT(NOM)}$ is to be enabled in MR1, the ODT input signal must be statically held LOW. In all cases, the ODT input signal remains static until the power up initialization sequence is finished, including the expiration of tDLLK and tZQinit.
5. After CKE is registered HIGH, wait a minimum of RESET CKE EXIT time, tXPR, before issuing the first MRS command to load mode register (tXPR = MAX (tXS; 5 × tCK).
6. Issue MRS command to load MR3 with all application settings, wait tMRD.
7. Issue MRS command to load MR6 with all application settings, wait tMRD.

8. Issue MRS command to load MR5 with all application settings, wait tMRD.
9. Issue MRS command to load MR4 with all application settings, wait tMRD. 10. Issue MRS command to load MR2 with all application settings, wait tMRD.
10. Issue MRS command to load MR1 with all application settings, wait tMRD.
11. Issue MRS command to load MR0 with all application settings, wait tMOD.
12. Issue a ZQCL command to start ZQ calibration.
13. Wait for tDLLK and tZQinit to complete.
14. The device will be ready for normal operation.

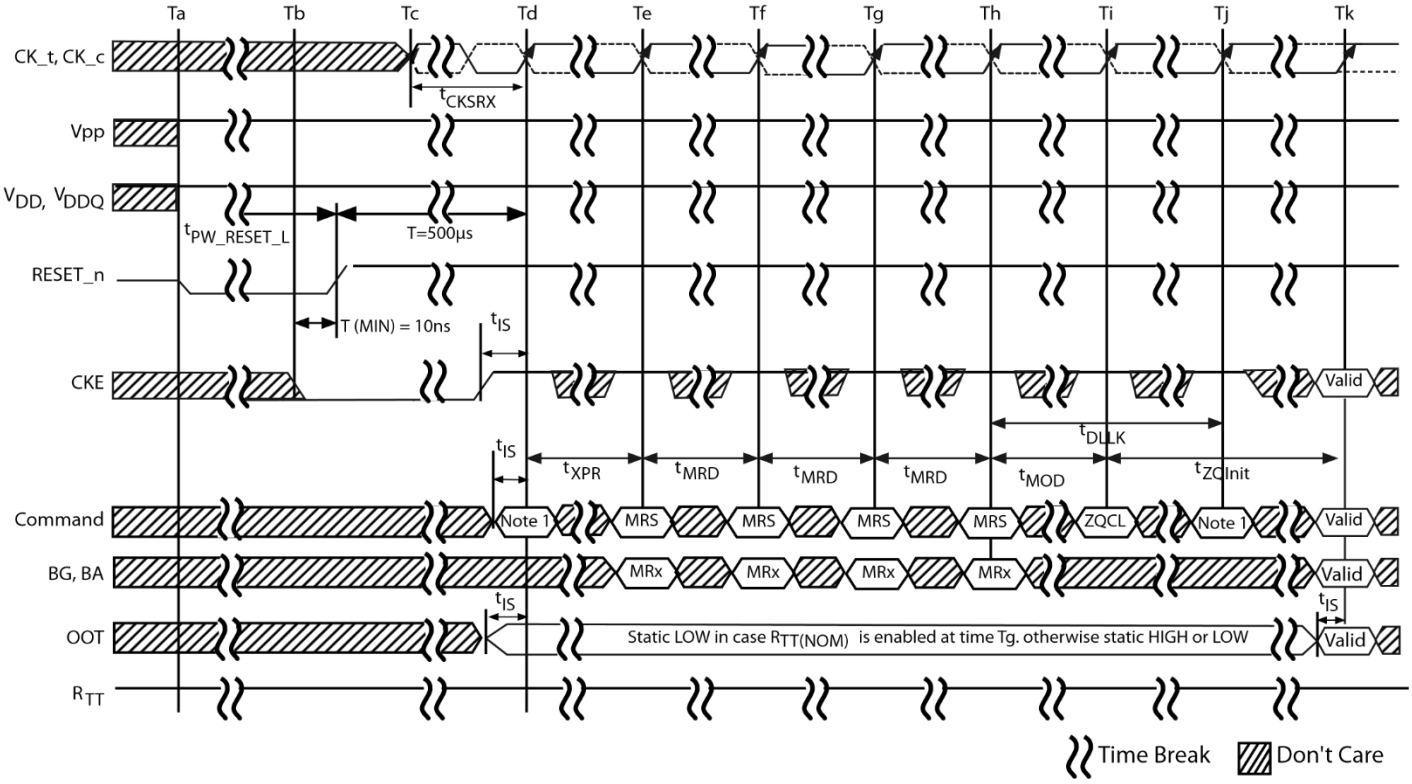

Figure 5 - Reset and Initialization Sequence at Power-On Ramping

Notes:

1. From time point Td until Tk, a DES command must be applied between MRS and ZQCL commands.
2. MRS commands must be issued to all mode registers that have defined settings.
3. In general, there is no specific sequence for setting the MRS locations (except for dependent or co-related features such as ENABLE DLL in MR1 prior to RESET DLL in MR0, for example.)
4. TEN is not shown; however, it is assumed to be held to LOW.

10.3 Reset with Stable Power

The following sequence is required for RESET at no power interruption initialization:

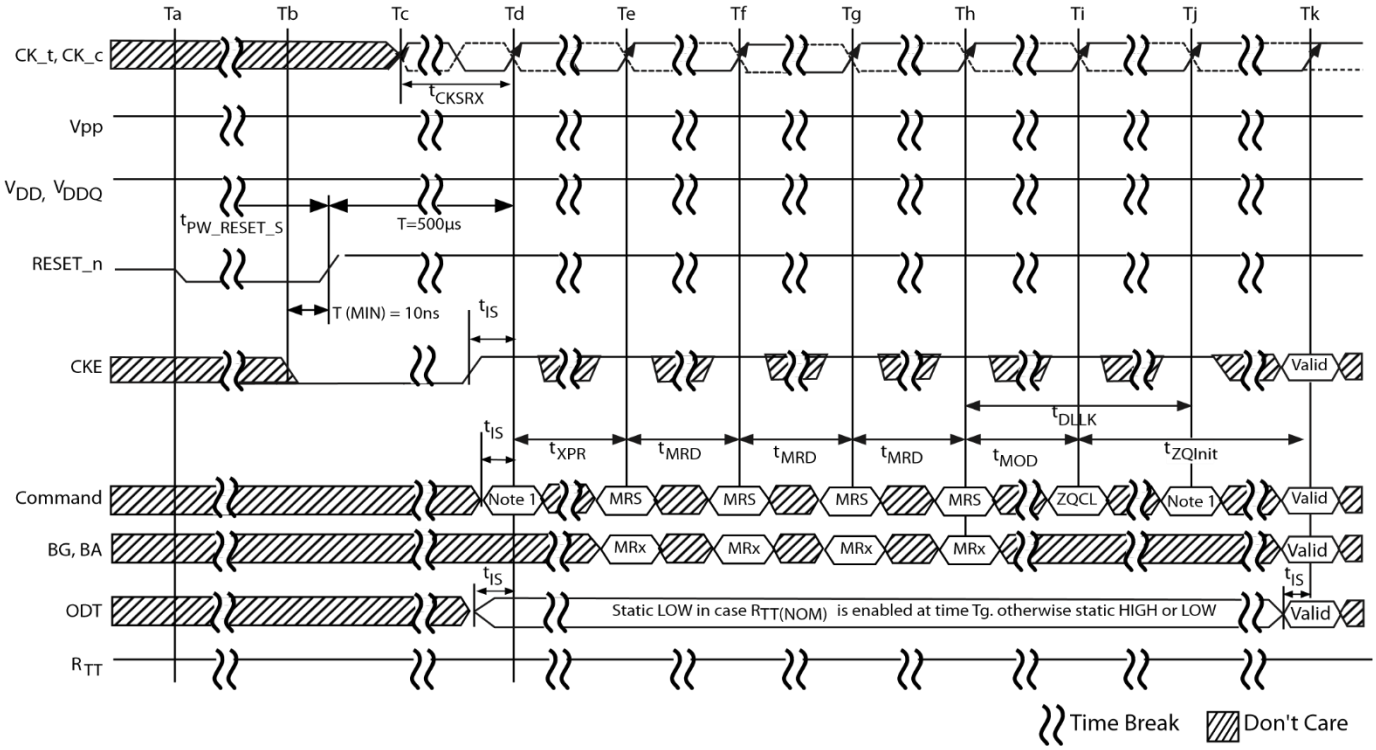

Figure 6 - Reset with Stable Power

Notes:

1. Assert RESET_n below 0.2 × V_{DD} any time a Reset is needed (all other inputs may be undefined). RESET_n must be maintained for a minimum of 100ns. CKE is pulled LOW before RESET_n is de-asserted (minimum time 10ns).
2. Follow Steps 2 through 7 in the Reset and Initialization Sequence at Power-on Ramping procedure.

When the Reset sequence is complete, the device is ready for normal operation.

3. From time point Td until Tk, a DES command must be applied between MRS and ZQCL commands.
4. MRS commands must be issued to all mode registers that have defined settings.
5. In general, there is no specific sequence for setting the MRS locations (except for dependent or co-related features such as ENABLE DLL in MR1 prior to RESET DLL in MR0, for example.)
6. TEN is not shown; however, it is assumed to be held to LOW.

10.4 Uncontrolled Power Down Sequence

In the event of an uncontrolled ramping down of the V_{PP} supply, V_{PP} is allowed to be less than V_{DD} provided the following conditions are met:

- Condition A: V_{PP} and V_{DD}/V_{DDQ} are ramping down (as part of turning off) from normal operating levels.
- Condition B: The amount that VPP may be less than VDD/VDDQ is less than or equal to 500mV.
- Condition C: The time V_{PP} may be less than V_{DD} is ≤ 10ms per occurrence with a total accumulated time in this state ≤ 100ms.
- Condition D: The time V_{PP} may be less than 2.0V and above V_{SS} while turning off is ≤ 15ms per occurrence with a total accumulated time in this state ≤ 150ms.

Note: In order to maintain non-volatility, all banks must be precharged and the STORA command issued before V_{PP} or V_{DD} falls below the specified minimum values.

11. MODE REGISTERS

11.1 Programing the Mode Registers

For application flexibility, various functions, features, and modes are programmable in seven Mode Registers, provided by the device, as user defined variables that must be programmed via a Mode Register Set (MRS) command. The Mode Registers are divided into various fields depending on the functionality and/or modes. Since the Mode Registers (MRn) do not have default values defined, contents of Mode Registers must be initialized and/or re-initialized, i.e. written, after power up and/or reset for proper operation. The contents of the Mode Registers can be altered by re-executing the MRS command during normal operation.

When programming the Mode Registers, even if the user chooses to modify only a subset of the MRS fields, all address fields within the accessed Mode Register must be redefined when the MRS command is issued. MRS commands do not affect the array contents which means these commands can be executed any time after power-up.

The MRS command cycle time, t_{MRD} is required to complete the write operation to the Mode Register and is the minimum time required between two MRS commands shown in Figure 7 - t_{MRD} Timing.

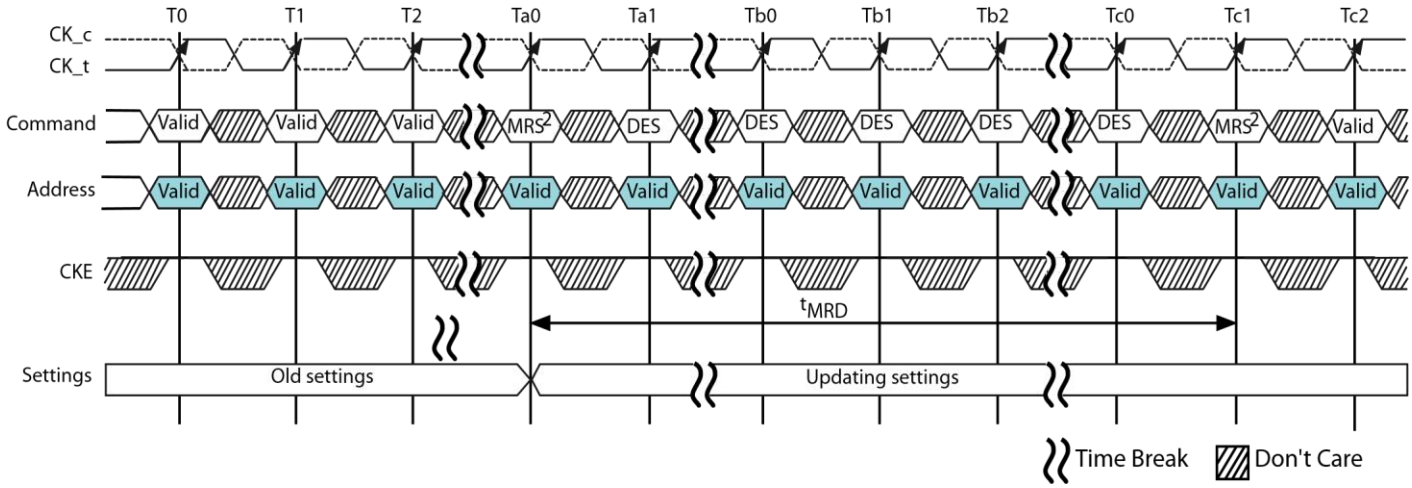

Figure 7 - t_{MRD} Timing

Notes:

1. This timing diagram depicts CA parity mode “disabled” case.
2. t_{MRD} applies to all MRS commands with the following exceptions:
3. Gear-down mode
4. CA parity mode
5. CAL mode
6. Per-DRAM addressability mode
7. V_{REFDQ} training value, V_{REFDQ} training mode, and V_{REFDQ} training range

Some of the Mode Register settings affect the address/command/control input functionality. In these cases, the next MRS command can be allowed when the function updating by current MRS command completes. This type of MRS command does not apply tMRD timing to next MRS command, however, these MRS command input cases have unique MR setting procedure, so refer to individual function descriptions. These commands include:

- Per Device Addressability mode
- V_{REFDQ} training value
- V_{REFDQ} training mode
- V_{REFDQ} training range

The MRS command to Non-MRS command delay, tMOD, is required for the device to update features, and is the minimum time required from an MRS command to a non-MRS command excluding DES is shown in Figure 8 - t_{MOD} Timing.

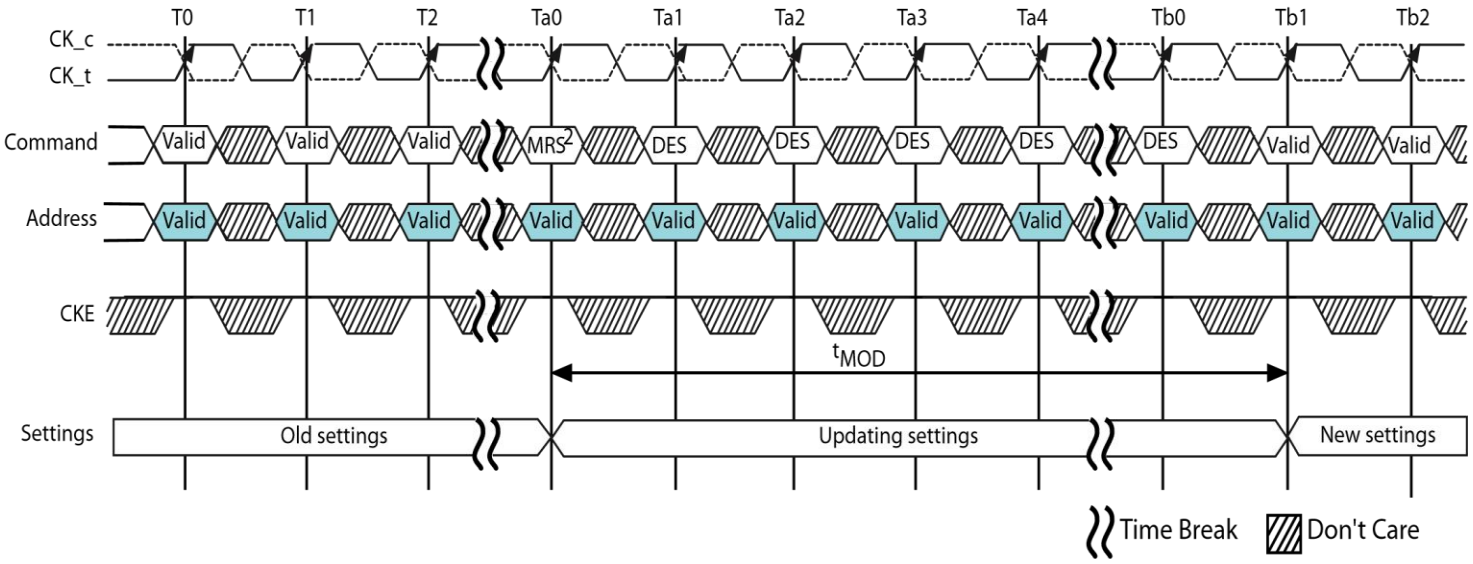

Figure 8 - t_{MOD} Timing

The Mode Register contents can be changed using the same command and timing requirements during normal operation as long as the device is in the idle state, i.e., all banks are in the precharged state with t_{RP} satisfied, all store operations are complete with t_{ST} satisfied, all data bursts are completed and CKE is high prior to writing into the Mode Register.

In some of the Mode Register setting cases, function updating takes longer than t_{MOD}. This type of MRS does not apply tMOD timing to next valid command, excluding DES. These MRS command input cases have unique mode register setting procedures, so refer to the individual function description.

11.2 Mode Register Structure

Table 44 – Mode Register 0 (MR0)

Mode Register	Operating Mode	Description	
BG1	RFU	Reserved, must be 0	
BG0, BA1:BA0	MR Select	000 = Not Supported 001 = Not Supported 010 = MR2 011 = Not Supported	100 = Not Supported 101 = Not Supported 110 = Not Supported 111 = Not Supported[1]
A13	NOMEM	0 = Disable NOMEM mode	1 = Enable NOMEM mode
A11:A9	WR/RTP[2,3]	000 = 10/5 001 = 12/6 010 = 14/7 011 = 16/8	100 = 18/9 101 = 20/10 110 = 24/12 111 = Reserved
A8 Reset	DLL	0 = No	1 = Yes
A7	TM	0 = Normal	1= Test
A12, A6:A4, A2	CAS Latency	00001 = 10CK	Only CL=10 is supported
A3	Read Burst	Type 0 = Sequential	1 = Not Supported[4]
A1:A0	Burst Length	00 = 8 (Fixed) 01 = BC4 or 8 (on the fly)	10 = BC4 (fixed) 11 = Reserved

[1] Reserved for Register control word setting. The device responds only to BG0, BA1:BA0=010. Device operation is not defined for any other setting.

[2] WR (write recovery for AUTOPRECHARGE) min in clock cycles is calculated by dividing tWR(in ns) by tCK(in ns) and rounding up to the next integer: WRmin[cycles] = Roundup(tWR[ns] / tCK[ns]). The WR value in the mode register must be programmed to be equal to or larger than WRmin. The programmed WR value is used with tRP to determine tDAL

[3] The table shows the encodings for Write Recovery and internal Read command to PRECHARGE command delay. For actual Write recovery timing please refer to AC timing table

[4] Read Burst Types other than Sequential are not supported. See Table 61 - Burst Length, Type and Order and for more information.

Table 45 – Mode Register 1 (MR1)

Mode Register	Operating Mode	Description	
BG1	RFU	Reserved, must be 0	
BG0, BA1:BA0	MR Select	000 = MR0 001 = MR1 010 = MR2 011 = MR3	100 = MR4 101 = MR5 110 = MR6 111 = RCW[1]
A13	MEM	Reserved, must be 0	-
A12	QOFF[2]	0 = Output buffer enabled	1 = Output buffer disabled
A11	TDQS Enable	0 = Disabled	1 = Enabled
A10:A8	$R_{TT(NOM)}$	000 = $R_{TT(NOM)}$ Disable Only 001 = Not Supported 010 = Not Supported 011 = Not Supported	100 = Not Supported 101 = Not Supported 110 = Not Supported 111 = Not Supported
A7	Write Leveling Enable	0 = Disabled	1 = Enabled
A6:A5	RFU	Reserved, must be 00	-
A4:A3	Additive Latency	Not supported, must be 00[3]	= 0 (AL disabled)
A2:A1	Output driver impedance control	00 = RZQ/7 01 = RZQ/5	10 = RZQ/6 11 = Reserved
A0	DLL Enable	0 = Disabled[4]	1 = Enabled

[1] Reserved for Register Control Word setting. The device ignores MR command with BG0, BA1;BA0=111 and doesn't respond. When RFU MRS code setting is set, device operation is not defined.
[2] Outputs disabled - DQs, DQS_t, DQS_c
[3] These features are disabled. Any attempt to change these bits will be ignored
[4] States reversed to "0 as Disable" with respect to DDR3

Table 46 – Mode Register 2 (MR2)

Mode Register	Operating Mode	Description	
BG1	RFU	Reserved, must be 0	
BG0, BA1:BA0	MR Select	000 = MR0 001 = MR1 010 = MR2 011 = MR3	100 = MR4 101 = MR5 110 = MR6 111 = RCW[1]
A13	TRR Mode	Not supported, must be 0[2]	0 = Disabled
A12	Write CRC	Not supported, must be 0[2]	0 = Disabled
A11:A9	$R_{TT(WR)}$	000 = Dynamic ODT off	-
A8:A2	T_{RR} Mode - BG*n* control	0 = Disabled	1 = Enabled
A7:A6	Low Power Array Self-Refresh	Reserved, must be 00[2]	-
A5:A3	CAS Write Latency (CWL)	000 = 9 only	CWL = 9 only
A1:A0	T_{RR} Mode - BA*n* control	Not supported, must be 00[2]	-

Table 47 – Mode Register 3 (MR3)

Mode Register	Operating Mode	Description	
BG1	RFU	Reserved, must be 0	-
BG0, BA1:BA0	MR Select	000 = MR0 001 = MR1 010 = MR2 011 = MR3	100 = MR4 101 = MR5 110 = MR6 111 = RCW[3]
A13	RFU	Reserved, must be 0	-
A12:A11	MPR Read Format	00 = Serial 01 = Not Supported[4]	10 = Not Supported[4] 11 = Not Supported[4]
A10:A9	Write CMD Latency when DM is enabled	00 = 4CK 01 = Not Supported[4]	10 = Not Supported[4] 11 = Reserved
A8	Refresh command executes Store All	0 = Disabled	1 = Enabled

[1] Reserved for Register Control Word setting, the device ignores MR command with BG0, BA1;BA0=111 and doesn't respond. When RFU MR code setting is set, device operation is not defined.
[2] These features are disabled. Any attempt to change these bits will be ignored
[3] Reserved for Register Control Word setting, the device ignores MR command with BG0, BA1;BA0=111 and doesn't respond. When RFU MR code setting is set, device operation is not defined.
[4] These features are disabled. Any attempt to change these bits will be ignored

Mode Register	Operating Mode	Description	
A7:A6	Store all bank staggering	00 = 2 banks 01 = 4 banks	10 = 8 banks 11 = 16 banks
A5	Temperature sensor readout	Not supported, must be 0[1]	0 = Disabled
A4	Per Device address-ability	0 = Disabled	1 = Enabled
A3	Gear-down mode	Not supported, must be 0[1]	0 = Disabled
A2	MPR Operation	0 = Normal	1 = Dataflow from/to MPR
A1:A0	MPR Page selection	00 = Page 0 01 = Page 1	10 = Page 2 11 = Page 3

Table 48 – MPR Page 0 (Training Pattern)

Address	MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Note
BA1:BA0	00 = MPR0	0	1	0	1	0	1	0	1	Read/Write (default value)
	01 = MPR1	0	0	1	1	0	0	1	1	
	10 = MPR2	0	0	0	0	1	1	1	1	
	11 = MPR3	0	0	0	0	0	0	0	0	

Table 49 – MPR Page 1 (Not Defined)

Address	MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Note
BA1:BA0	00 = MPR0	X	X	X	X	X	X	X	X	Read/Write (default value)
	01 = MPR1	X	X	X	X	X	X	X	X	
	10 = MPR2	X	X	X	X	X	X	X	X	
	11 = MPR3	X	X	X	X	X	X	X	X	

[1] These features are disabled. Any attempt to set non-supported values will be ignored

Table 50 – MPR Page 2 (MRS Readout)

Address	MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Note
BA1:BA0	00 = MPR0	RFU	RFU	RTT(WR)	Temperature Sensor Status		CRC Write Enable	RTT(WR)		Read Only
		-	-	MR2	-	-	MR2	MR2		
		-	-	A11	0	1	A12	A10	A9	
	01 = MPR1	VREFDQ	VREF Training Value						Gear Down Enable	
		MR6	MR6						MR3	
		A6	A5	A4	A3	A2	A1	A0	A3	
	10 = MPR2	CAS Latency					CAS Write Latency			
		MR0					MR2			
		A6	A5	A4	A2	A12	A5	A4	A3	
	11 = MPR3	RTT(NOM)			RTT(PARK)			Driver Impedance		
		MR1			MR5			MR2		
		A10	A9	A8	A8	A7	A6	A2	A1	

Table 51 – MPR Page 3 (Vendor Use Only)

Address	MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Note
BA1:BA0	00 = MPR0	X	X	X	X	X	X	X	X	Read/Write (default value)
	01 = MPR1	X	X	X	X	X	X	X	X	
	10 = MPR2	X	X	X	X	X	X	X	X	
	11 = MPR3	X	X	X	X	X	X	X	X	

Table 52 – Mode Register 4 (MR4)

Mode Register	Operating Mode	Description	
BG1	RFU	Reserved, must be 0	-
BG0, BA1:BA0	MR Select	000 = MR0 001 = MR1 010 = MR2 011 = MR3	100 = MR4 101 = MR5 110 = MR6 111 = RCW[1]
A13	RFU	Reserved, must be 0	-
A12	Write Preamble	Not Supported, must be 0[2]	1 CK
A11	Read Preamble	Not Supported, must be 0[2]	1 CK
A10	Read Preamble Training Mode	0 = Disabled	1 = Enabled
A9	Self-refresh Abort	Not Supported, must be 0[2]	0 = Disabled
A8:A6	CS to CMD / ADDR Latency Mode (cycles)	Not Supported, must be 000	000 = Disabled
A5	RFU	Reserved, must be 0	
A4	Internal V_{REF} Monitor	0 = Disabled	1 = Enabled
A3	Temperature Controlled Refresh Mode	Not Supported, must be 0[2]	0 = Normal
A2	Temperature Controlled Refresh Range	Not Supported, must be 0[2]	1 = Disabled
A1	Maximum Power Savings Mode	Not Supported, must be 0[2,3]	0 = Disabled
A0	RFU	Reserved, must be 0	-

[1] Reserved for Register Control Word setting. The ST-DDR4 device ignores the MR command with BG0, BA1;BA0=111 and doesn't respond. When RFU MR code is set, the device's operation is not defined.
[2] These features are disabled. Any attempt to change these bits will be ignored
[3] See "Table 3 - JESD79-4A Unsupported Feature Options"

Table 53 – Mode Register 5 (MR5)

Mode Register	Operating Mode	Description	
BG1	RFU	Reserved, must be 0	
BG0, BA1:BA0	MR Select	000 = MR0 001 = MR1 010 = MR2 011 = MR3	100 = MR4 101 = MR5 110 = MR6 111 = RCW[1]
A13	RFU	Reserved, must be 0	-
A12	Read DBI	Not Supported, must be 0[2]	0 = Disabled
A11	Write DBI	Not Supported, must be 0[2]	0 = Disabled
A10	Data Mask	0 = Disabled	1 = Enabled
A9	CA Parity Persistent Error	Not Supported, must be 0[2]	0 = Disabled
A8:A6	$R_{TT(PARK)}$	000 = $R_{TT(park)}$ Disable 001 = RZQ/4 010 = RZQ/2 011 = RZQ/6	100 = RZQ/1 101 = RZQ/5 110 = RZQ/3 111 = RZQ/7
A5	ODT Input Buffer during Power Down Mode	0 = Buffer is activated	1 = Buffer is deactivated
A4	C/A Parity Error Status	Not Supported, must be 0[2]	0 = Clear
A3	CRC Error Clear	Not Supported, must be 0[2]	0 = Clear
A2:A0	C/A Parity Latency Mode	Not Supported, must be 000[2]	0 = Disabled

[1] Reserved for Register Control Word setting. The ST-DDR4 device ignores the MR command with BG0, BA1;BA0=111 and doesn't respond. When RFU MR code is set, the device's operation is not defined.
[2] These features are disabled. Any attempt to change these bits will be ignored

Table 54 – Mode Register 6 (MR6)

Mode Register	Operating Mode	Description	
BG1	RFU	Reserved, must be 0	
BG0, BA1:BA0	MR Select	000 = MR0 001 = MR1 010 = MR2 011 = MR3	100 = MR4 101 = MR5 110 = MR6 111 = RCW[1]
A13	RFU	Reserved, must be 0	-
A12:A10	tCCD_L	See Table 56 – tCCD_L	-
A9	RFU	Reserved, must be 0	-
A8	RFU	Reserved, must be 0	-
A7	V_{REFDQ} Training Enable	0 = Disabled (Normal Operation)	1 = Enabled
A6	VREFDQ Training Range	0 = Range 1	1 = Range 2
A5:A0	VREFDQ Training Value	See Table 55 – VREFDQ Range and Levels	-

[1] Reserved for Register Control Word setting. The ST-DDR4 device ignores the MR command with BG0, BA1;BA0=111 and doesn't respond. When RFU MR code is set, the device's operation is not defined.

Table 55 – VREFDQ Range and Levels

A5:A0	Range1	Range 2
00 0000	60.00%	45.00%
00 0001	60.65%	45.65%
00 0010	61.30%	46.30%
00 0011	61.95%	46.95%
00 0100	62.60%	47.60%
00 0101	63.25%	48.25%
00 0110	63.90%	48.90%
00 0111	64.55%	49.55%
00 1000	65.20%	50.20%
00 1001	65.85%	50.85%
00 1010	66.50%	51.50%
00 1011	67.15%	52.15%
00 1100	67.80%	52.80%
00 1101	68.45%	53.45%
00 1110	69.10%	54.10%
00 1111	69.75%	54.75%
01 0000	70.40%	55.40%
01 0001	71.05%	56.05%
01 0010	71.70%	56.70%
01 0011	72.35%	57.35%
01 0100	73.00%	58.00%
01 0101	73.65%	58.65%
01 0110	74.30%	59.30%
01 0111	74.95%	59.95%
01 1000	75.60%	60.60%
01 1001	76.25%	61.25%

A5:A0	Range1	Range2
01 1010	76.90%	61.90%
01 1011	77.55%	62.55%
01 1100	78.20%	63.20%
01 1101	78.85%	63.85%
01 1110	79.50%	64.50%
01 1111	80.15%	65.15%
10 0000	80.80%	65.80%
10 0001	81.45%	66.45%
10 0010	82.10%	67.10%
10 0011	82.75%	67.75%
10 0100	83.40%	68.40%
10 0101	84.05%	69.05%
10 0110	84.70%	69.70%
10 0111	85.35%	70.35%
10 1000	86.00%	71.00%
10 1001	86.65%	71.65%
10 1010	87.30%	72.30%
10 1011	87.95%	72.95%
10 1100	88.60%	73.60%
10 1101	89.25%	74.25%
10 1110	89.90%	74.90%
10 1111	90.55%	75.55%
11 0000	91.20%	76.20%
11 0001	91.85%	76.85%
11 0010	92.50%	77.50%
11 0011 to 11 1111	Reserved	Reserved

Table 56 – tCCD_L

A12	A11	A10	tCCD_L(min) (CK)	tDLLK(min) (CK)	Note
0	0	0	4	597	≤ 1333Mbps
0	0	1	5		≤ 1866Mbps (1600/1866 Mbps)
0	1	0	6	768	≤ 2400Mbps (2133/2400 Mbps)
0	1	1	7	1028	≤ Not Supported
1	0	0	8		≤ Not Supported
1	0	1	Reserved		
1	1	0			
1	1	1			

11.3 MPR Reads

MPR reads are supported using BL8 and BC4 modes. Burst length on-the-fly is not supported for MPR reads. READ commands for BC4 are supported with a starting column address of A[2:0] = 000 or 100. After power-up, the content of MPR Page 0 has the default values, which are defined in "Table 48 – MPR Page 0 (Training Pattern)". MPR page 0 can be rewritten via an MPR WRITE command. The device maintains the default values unless it is rewritten by the ST-DDR4 controller. If the ST-DDR4 controller does overwrite the default values (Page 0 only), the device will maintain the new values unless re-initialized or there is power loss.

Timing in MPR mode:

- Reads (back-to-back) from Page 0 may use tCCD_S or tCCD_L timing between READ commands
- Reads (back-to-back) from Pages 1, 2, or 3 may not use tCCD_S timing between READ commands; tCCD_L must be used for timing between READ commands.
  The following steps are required to use the MPR to read out the contents of a mode register (MPR Page x, MPRy).

1. The DLL must be locked if enabled.
2. Precharge all; wait until tRP is satisfied.
3. MRS command to MR3[A2] = 1 (Enable MPR data flow), MR3[A12:A11] = MPR read format, and MR3[A1:A0] MPR page.
   MR3[12:11] MPR read format:
   00 = Serial read format
   01 = Not Supported
   10 = Not Supported
   11 = RFU

MR3[1:0] MPR page:
00 = MPR Page 0
01 = MPR Page 1
10 = MPR Page 2
11 = MPR Page 3

4. tMRD and tMOD must be satisfied.
5. Redirect all subsequent READ commands to specific MPRx location.
6. Issue RD or RDA command.
   BA1 and BA0 indicate MPRx location:
   00 = MPR0
   01 = MPR1
   10 = MPR2
   11 = MPR3
   A12/BC = 0 or 1; BL8 or BC4 fixed-only, BC4 OTF not supported.
   If BL = 8 and MR0[A1:A0] = 01, A12/BC must be set to 1 during MPR READ commands.
   A2 = burst-type dependent:
   BL8: A2 = 0 with burst order fixed at 0, 1, 2, 3, 4, 5, 6, 7
   BL8: A2 = 1 not allowed
   BC4: A2 = 0 with burst order fixed at 0, 1, 2, 3, T, T, T, T
   BC4: A2 = 1 with burst order fixed at 4, 5, 6, 7, T, T, T, T A[1:0] = 00, data burst is fixed nibble start at 00. Remaining address inputs, including A10, and BG1 and BG0 are “Don’t Care.”
7. After RL = CL, the device bursts data from MPRx location; MPR readout format determined by MR3[A12,A11,A1,A0].
8. Steps 5 through 7 may be repeated to read additional MPRx locations.
9. After the last MPRx READ burst, t_{MPRR} must be satisfied prior to exiting.
10. Issue MRS command to exit MPR mode; MR3[A2] = 0.
11. After the t_{MOD} sequence is complete, the device is ready for normal operation

11.4 MPR Readout Format

Only the serial read data format is supported.

11.5 MPR Readout Serial Format

The serial format is required when enabling the MPR function to read out the contents of an MRx, temperature sensor status, and the command address parity error frame. However, data bus calibration locations (four 8-bit registers) can be programmed to read out any of the three formats. The device is required to drive associated strobes with the read data similar to normal operation (such as using MRS preamble settings).
Serial format implies that the same pattern is returned on all DQ lanes, as shown the table below, which uses values programmed into the MPR via [7:0] as 0111 1111.

Table 57 - MPR Readout Serial Format (x8)

Serial	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ0	0	1	1	1	1	1	1	1
DQ1	0	1	1	1	1	1	1	1
DQ2	0	1	1	1	1	1	1	1
DQ3	0	1	1	1	1	1	1	1
DQ4	0	1	1	1	1	1	1	1
DQ5	0	1	1	1	1	1	1	1
DQ6	0	1	1	1	1	1	1	1
DQ7	0	1	1	1	1	1	1	1

Table 58 – MPR Readout Serial Format (x16)

Serial	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ0	0	1	1	1	1	1	1	1
DQ1	0	1	1	1	1	1	1	1
DQ2	0	1	1	1	1	1	1	1
DQ3	0	1	1	1	1	1	1	1
DQ4	0	1	1	1	1	1	1	1
DQ5	0	1	1	1	1	1	1	1
DQ6	0	1	1	1	1	1	1	1
DQ7	0	1	1	1	1	1	1	1
DQ8	0	1	1	1	1	1	1	1
DQ9	0	1	1	1	1	1	1	1
DQ10	0	1	1	1	1	1	1	1
DQ11	0	1	1	1	1	1	1	1
DQ12	0	1	1	1	1	1	1	1
DQ13	0	1	1	1	1	1	1	1
DQ14	0	1	1	1	1	1	1	1
DQ15	0	1	1	1	1	1	1	1

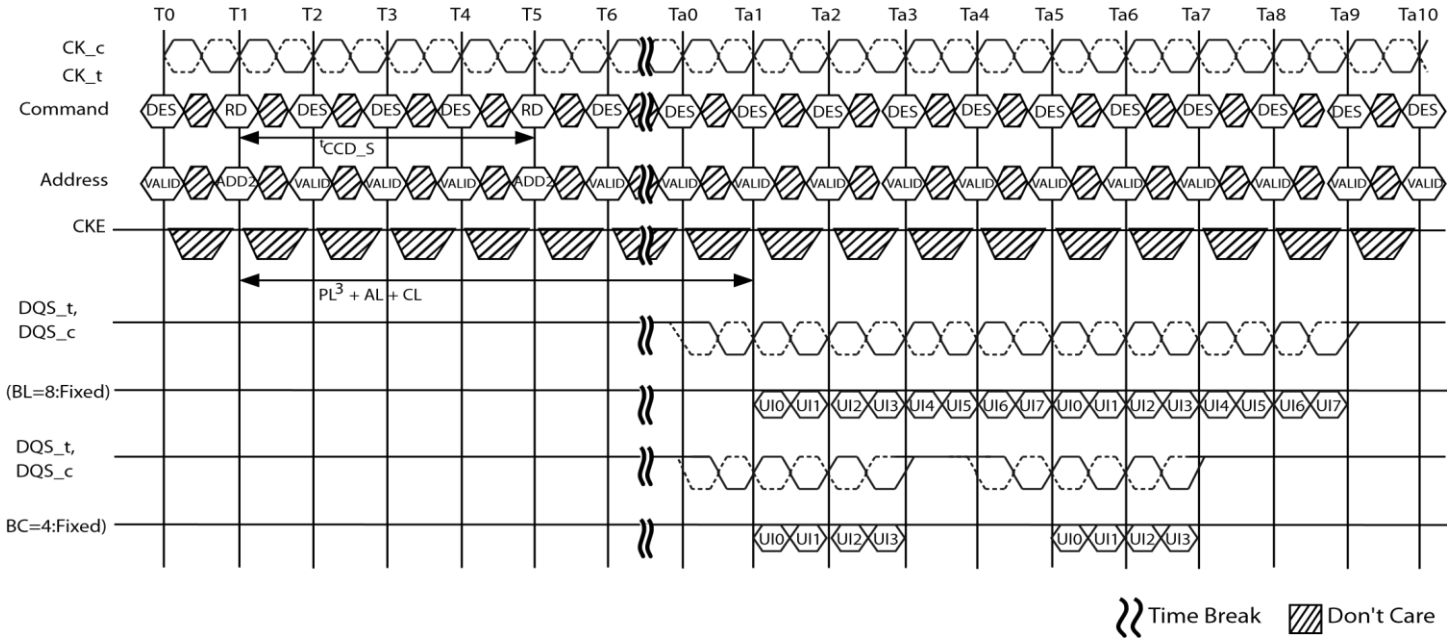

Figure 9 - MPR Read Timing

Notes:

1. tCCD_S = 4, Read Preamble = 1tCK
2. Address setting:
   - A[1:0] = “00”b (data burst order is fixed starting at nibble, always 00b here)
   - A[2]= “0”b (For BL=8, Burst order is fixed at 0,1,2,3,4,5,6,7)
   - (For BC=4, burst order is fixed at 0,1,2,3,T,T,T,T)
   - BA1 and BA0 indicate the MPR location
   - A10 and other address pins are don’t care including BG1 and BG0. A12 is don’t care when MR0 A[1:0] = “00” or “10”, and must be ‘1’b when MR0 A[1:0] = “01”

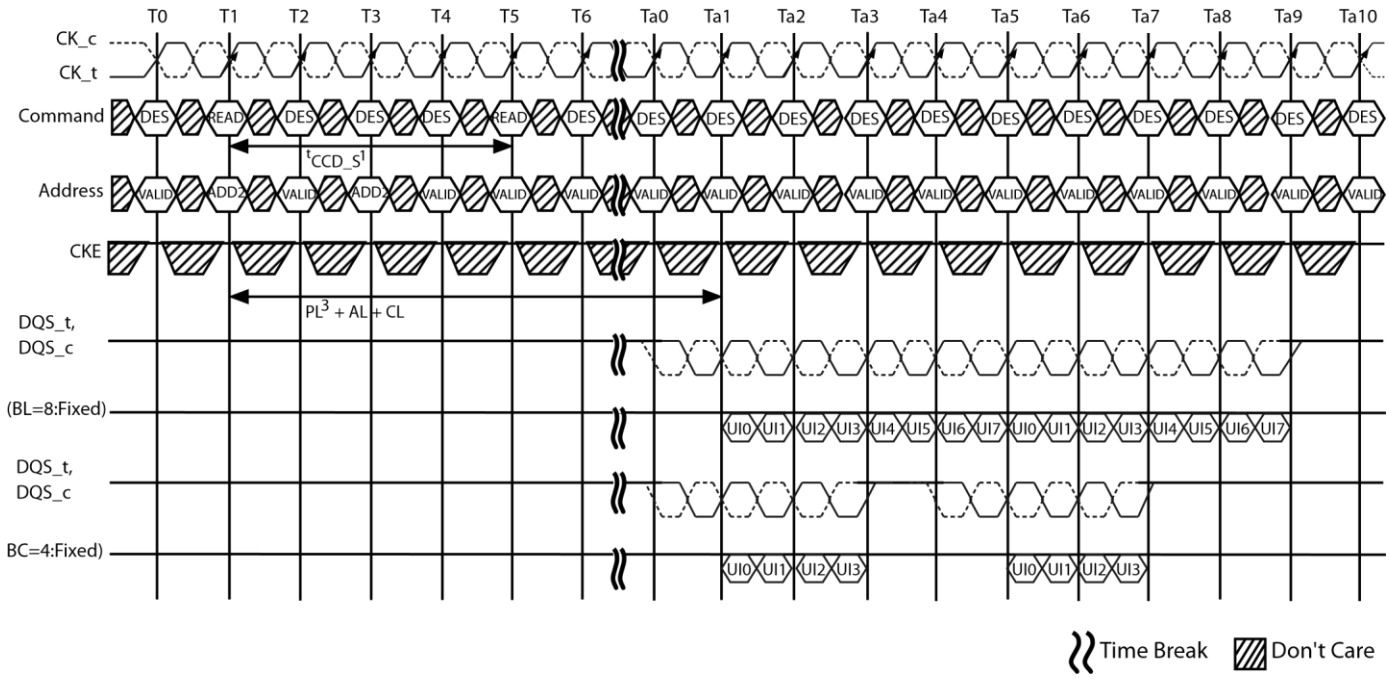

Figure 10 - MPR Back-to-Back Read Timing

Notes:

1. tCCD_S = 4, Read Preamble = 1tCK
2. Address setting:
   - A[1:0] = “00”b (data burst order is fixed starting at nibble, always 00b here)
   - A[2]= “0”b (For BL=8, Burst order is fixed at 0,1,2,3,4,5,6,7)
   - (For BC=4, burst order is fixed at 0,1,2,3,T,T,T,T)
   - BA1 and BA0 indicate the MPR location
   - A10 and other address pins are don’t care including BG1 and BG0. A12 is don’t care when MR0 A[1:0] = “00” or “10”, and must be ‘1’b when MR0 A[1:0] = “01”

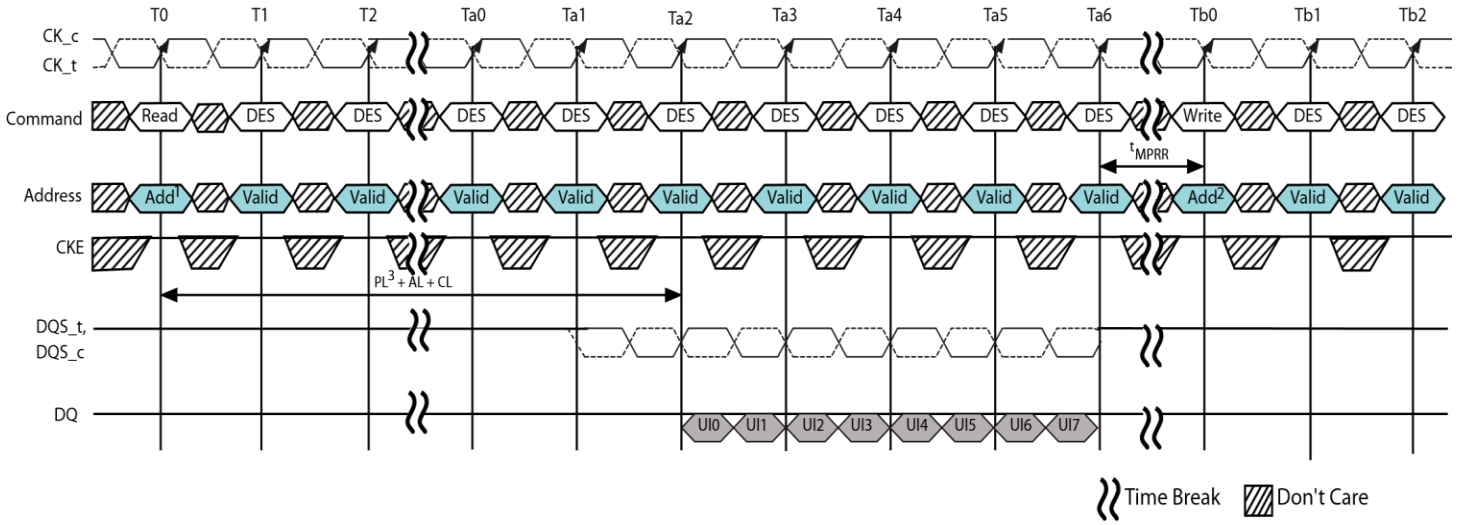

Figure 11 - MPR Read-to-Write Timing

Notes:

1. Address setting:
   A[1:0] = 00b (data burst order is fixed starting at nibble, always 00b)
   A2 = 0b (For BL=8, Burst order is fixed at 0,1,2,3,4,5,6,7)
   BA1 and BA0 indicate the MPR location A10 and other address pins are don't care including BG1 and BG0. A12 is don't care when MR0 A[1:0] = 00 and must be 1b when MR0 A[1:0] = 01
2. Address setting:
   BA1 and BA0 indicate the MPR location A[7:0] = data for MPR
   BA1 and BA0 indicate the MPR location
   A10 and other address pins are "Don't Care"

11.6 MPR Writes

MPR access mode allows 8-bit writes to the MPR location using the address bus A[7:0]. The device will maintain the new written values unless re-initialized or there is power loss.
The following steps are required to use the MPR to write to mode register MPR Page 0, MPRx.

1. The DLL must be locked if enabled.
2. Precharge all; wait until tRP is satisfied.
3. MRS command to MR3[A2] = 1 (enable MPR data flow) and MR3[A1:A0] = 00 (MPR Page 0); 01, 10, and 11 are not allowed.
4. tMRD and tMOD must be satisfied.
5. Redirect all subsequent WRITE commands to specific MPRx location.
6. Issue WR or WRA command: BA1 and BA0 indicate MPRx location
   00 = MPR0
   01 = MPR1
   10 = MPR2
   11 = MPR3

A[7:0] = data for MPR Page 0, mapped A[7:0] to UI[7:0].
Remaining address inputs, including A10, and BG1 and BG0 are “Don’t Care.”

7. tWR_MPR must be satisfied to complete MPR WRITE.
8. Steps 5 through 7 may be repeated to write additional MPRx locations.
9. After the last MPRx WRITE, tMPRR must be satisfied prior to exiting.
10. Issue MRS command to exit MPR mode; MR3[A2] = 0.
11. When the tMOD sequence is completed, the device is ready for normal operation from the core (such as ACT).

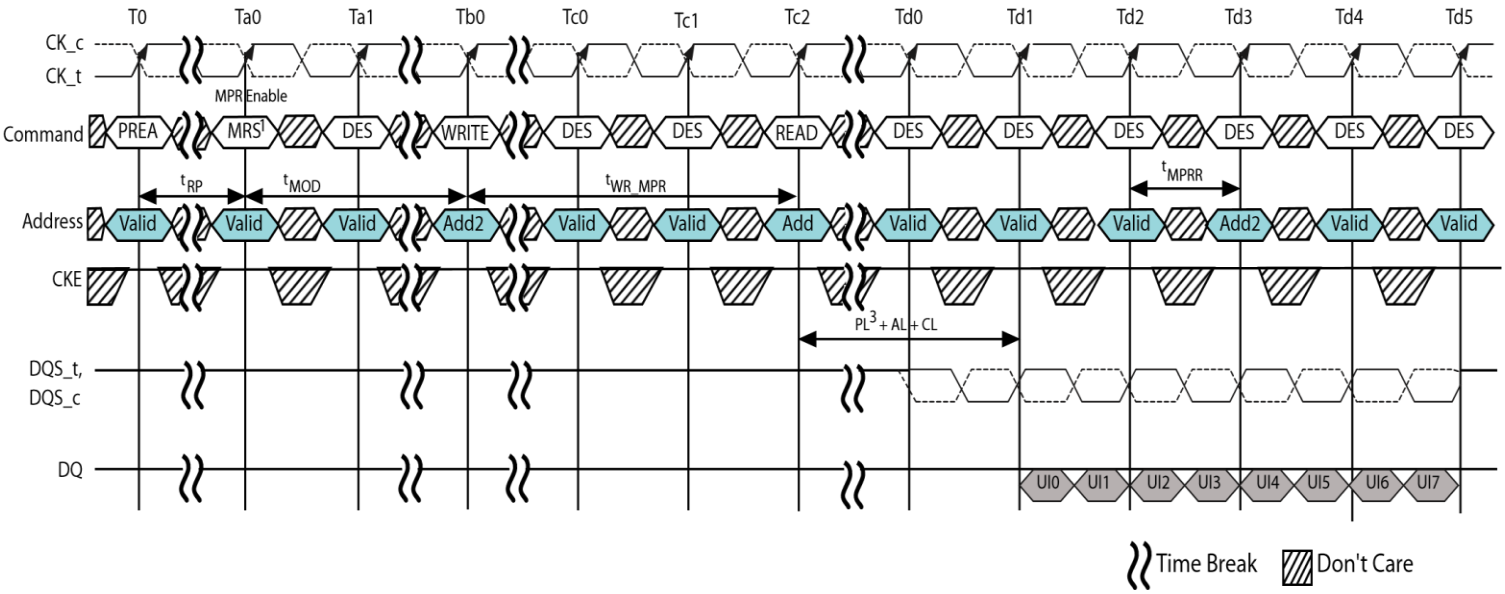

Figure 12 - MPR Write and Write-to-Read Timing

Notes:

1. Multipurpose register read/write enable (MR3 A2 = 1).
2. Address setting:
   - BA1 and BA0 indicate the MPR location
   - A10 and other address pins are “Don’t Care”
3. Parity latency (PL) is added to data output delay when CA parity latency mode is enabled.

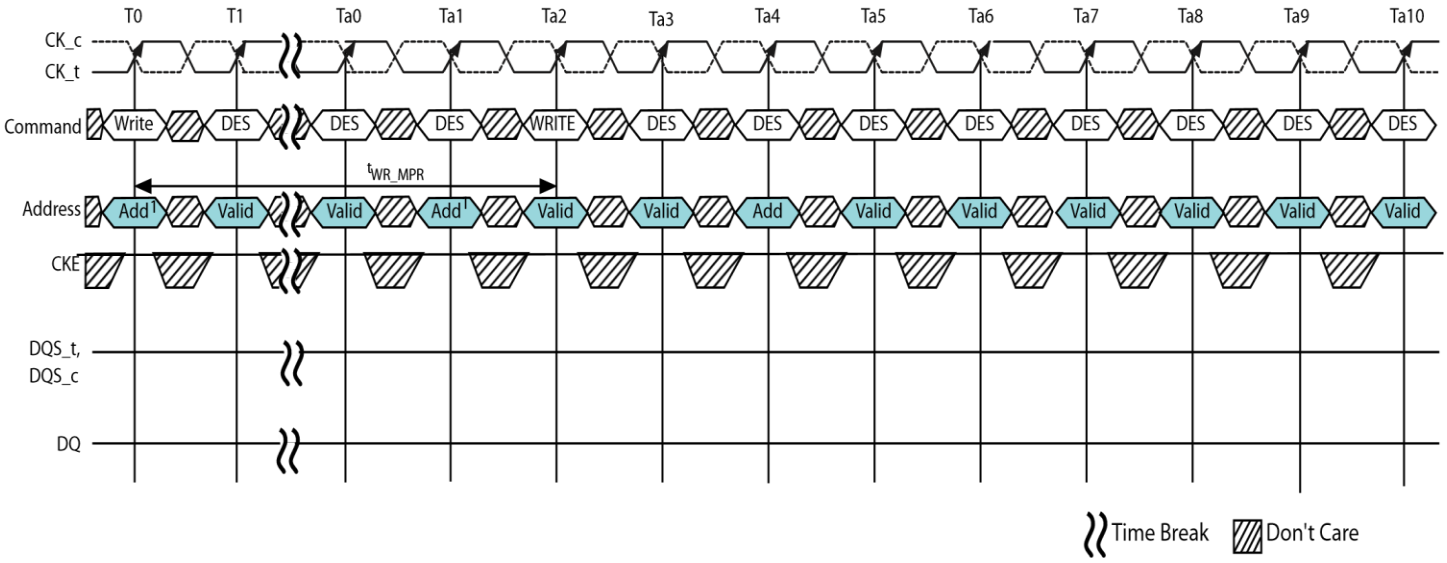

Figure 13 - MPR Back-to-Back Write Timing

Notes:

1. Address setting:
   - BA1 and BA0 indicate the MPR location
   - A[7:0] = data for MPR
   - A10 and other address pins are “Don’t Care”

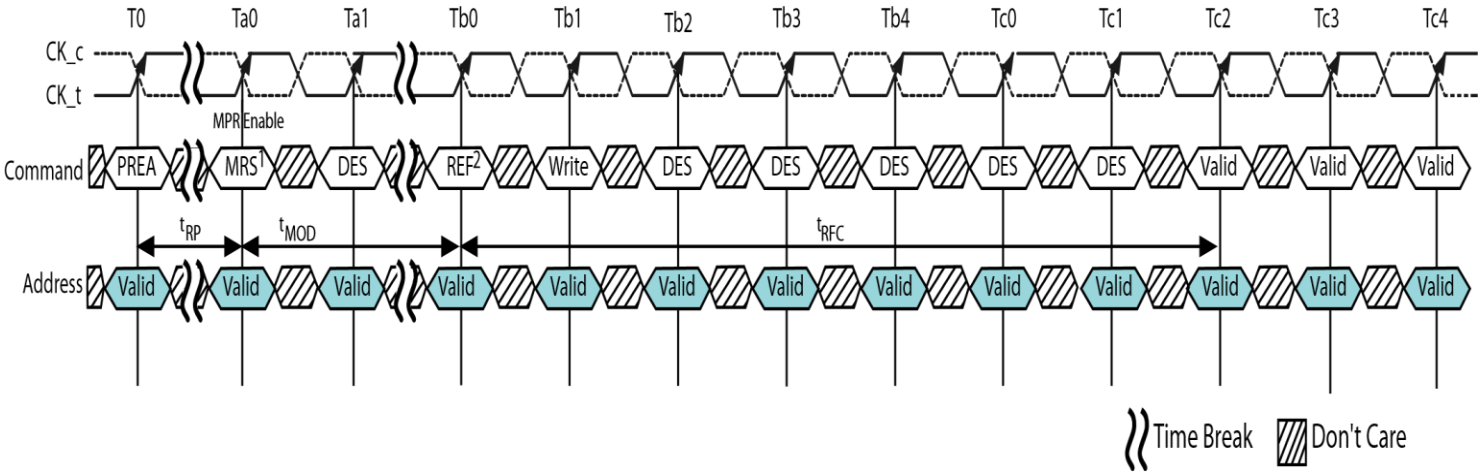

Figure 14 - MPR Refresh Timing

Notes:

1. Multipurpose registers read/write enable (MR3 A2 = 1). Redirect all subsequent read and writes to MPR locations.
2. 1x refresh is only allowed when MPR mode is enabled.

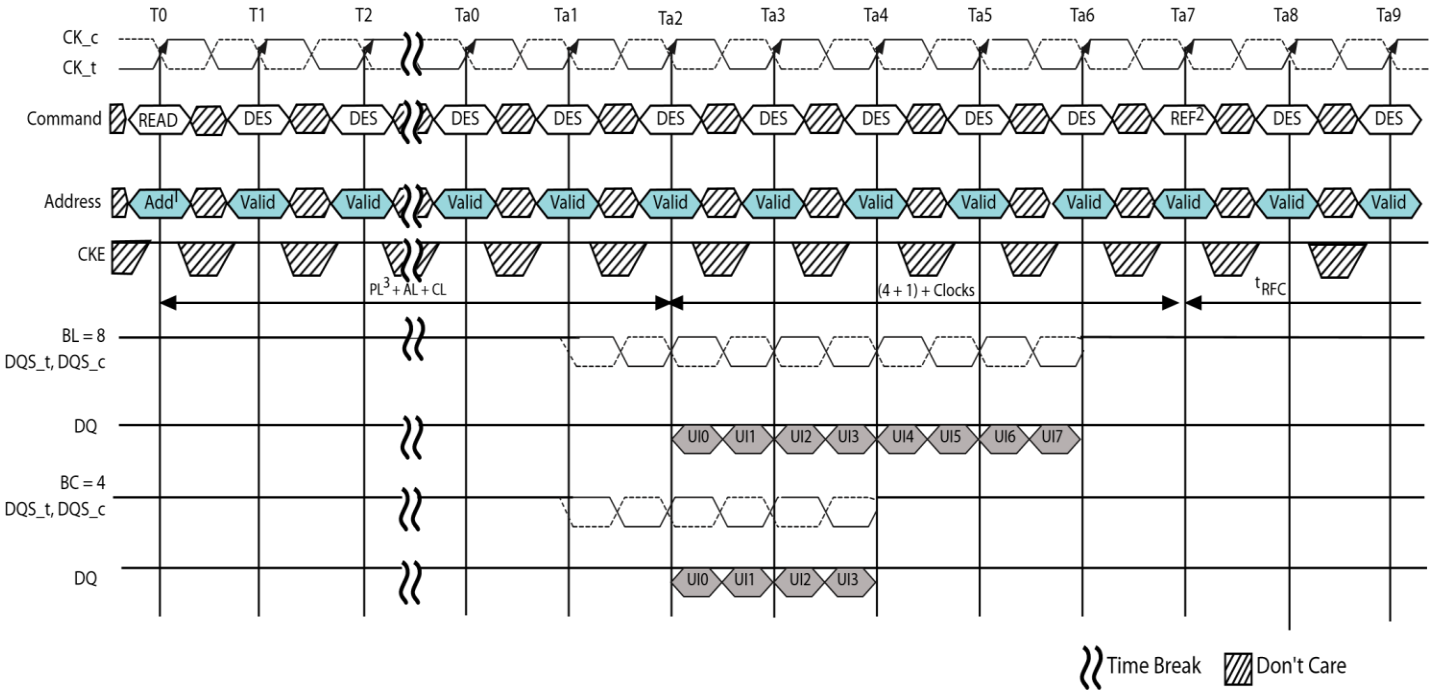

Figure 15 - MPR Read-to-Refresh Timing

Notes:

1. Address setting
   - A[1:0] = 00b (data burst order is fixed starting at nibble, always 00b here)
   - A2 = 0b (For BL=8, Burst order is fixed at 0,1,2,3,4,5,6,7)
   - BA1 and BA0 indicate the MPR location
   - A10 and other address pins are don't care including BG1 and BG0. A12 is don't care when MR0 A[1:0] = 00 or 10, and must be 1b when MR0 A[1:0] = 01
2. 1x Refresh is only allowed when MPR mode is enabled.

12. COMMAND DESCRIPTIONS

Table 59 – CKE Truth Table

Current State[1]	CKE		Command (N)[2] AS_n, CAS_n, E_n, CS_n	Action	Note
	Previous Cycle[3] (N-1)	Current Cycle[3] (N)			
Power Down	L	L	X	Maintain Power Down	14,15
	L	H	DESELECT	Power Down Exit	11,14
Self-Refresh	L	L	X	Maintain Self-Refresh	15,16
	L	H	DESELECT	Self-Refresh Exit	8, 12, 16
Bank(s) Active	H	L	DESELECT	Active Power Down Entry	11, 13, 14
Reading	H	L	DESELECT	Power Down Entry	11, 13, 14, 17
Writing	H	L	DESELECT	Power Down Entry	11, 13, 14, 17
Precharging	H	L	DESELECT	Power Down Entry	11, 13, 14, 17
Refreshing	H	L	DESELECT	Precharge Power Down Entry	11
All Banks Idle	H	L	DESELECT	Precharge Power Down Entry	11, 13, 14, 18
	H	L	Refresh	Self-Refresh Entry	9, 13, 18
For more details with all signals See "**Table 60 - Command Truth Table**".					10

Notes for CKE Truth Table:

4. All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
5. During any CKE transition (registration of CKE H->L or CKE L->H), the CKE level must be maintained until 1nCK prior to tCKEmin being satisfied (at which time CKE may transition again).
6. DESELECT and NOP are defined in "Table 60 - Command Truth Table".
7. On Self-Refresh Exit DESELECT commands must be issued on every clock edge occurring during the tXS period. Read commands may be issued only after tXSDLL is satisfied.
8. Self-Refresh mode can only be entered from the All Banks Idle state.
9. Must be a legal command as defined in "Table 60 - Command Truth Table".
10. Valid commands for Power-Down Entry and Exit are DESELECT only.

[1] Current state is defined as the state of the ST-DDR4 device immediately prior to clock edge N
[2] Command (N) is the command registered at clock edge N, and Action (N) is a result of Command (N)
[3] CKE (N) is the logic state of CKE at clock edge N; CKE (N-1) was the state of CKE at the previous clock edge

11. Valid commands for Self-Refresh Exit are DESELECT only
12. Self-Refresh cannot be entered during Read or Write operations.
13. The Power-Down does not perform any refresh operations.
14. “X” means “don’t care” (including floating around VREF) in Self-Refresh and Power-Down. It also applies to Address pins.
15. VPP and VREFCA must be maintained during Self-Refresh operation. The first Write operation or first Write Leveling Activity may occur after tXS time after exit from Self-refresh
16. If all banks are closed at the conclusion of the READ, WRITE or PRECHARGE command, then Precharge Power-Down is entered, otherwise Active Power-Down is entered.
17. “Idle state” is defined as all banks are closed (tRP, tDAL, etc. satisfied), no data bursts are in progress, CKE is high, and all timings from previous operations are satisfied (tMRD, tMOD, tRFC, tZQinit, tZQoper, etc.) as well as all Self-Refresh exit and Power-Down Exit parameters are satisfied (tXS, tXP, etc.)

Table 60 - Command Truth Table

Function	Abbr	CKE[11]		CS_n	ACT_n	RAS_n	CAS_n /A15	WE_n /A14	BG0-BG1	BA0-BA1	A12/ BC_n	A13, A11	A10 /AP	A0-A6	Note
		PREV	CUR												
Mode Register Set	MRS	H	H	L	H	L	L	L	BG	BA	OP Code				
Refresh	REF	H	H	L	H	L	L	H	V	V	V	V	V	V	11
Self-refresh Entry	SRE	H	L	L	H	L	L	H	V	V	V	V	V	V	7, 9
Self-refresh Exit	SRX	L	H	H	X	X	X	X	X	X	X	X	X	X	7, 8, 9, 10
				L	H	H	H	H	V	V	V	V	V	V	
Single Bank Precharge	PRE	H	H	L	H	L	H	L	BG	BA	V	V	L	V	1
Precharge all Banks	PREA	H	H	L	H	L	H	L	V	V	V	V	H	V	
Bank Activate	ACT	H	H	L	L	V	Row Address (RA)		BG	BA	Row Address (RA)				
Write (Fixed BL8 or BC4)	WR	H	H	L	H	H	L	L	BG	BA	V	V	L	CA	
Write (BC4, on the Fly)	WRS4	H	H	L	H	H	L	L	BG	BA	L	V	L	CA	
Write (BL8, on the Fly)	WRS8	H	H	L	H	H	L	L	BG	BA	H	V	L	CA	
Write with Auto Precharge (Fixed BL8 or BC4)	WRA	H	H	L	H	H	L	L	BG	BA	V	V	H	CA	
Write with Auto Precharge (BC4, on the Fly)	WRAS4	H	H	L	H	H	L	L	BG	BA	L	V	H	CA	
Write with Auto Precharge (BL8, on the Fly)	WRAS8	H	H	L	H	H	L	L	BG	BA	H	V	H	CA	
Read (Fixed BL8 orBC4)	RD	H	H	L	H	H	L	H	BG	BA	V	V	L	CA	
Read (BC4, on the Fly)	RDS4	H	H	L	H	H	L	H	BG	BA	L	V	L	CA	
Read (BL8, on the Fly)	RDS8	H	H	L	H	H	L	H	BG	BA	H	V	L	CA	
Read with Auto Precharge (Fixed BL8 or BC4)	RDA	H	H	L	H	H	L	H	BG	BA	V	V	H	CA	

Function	Abbr	CKE[11]		CS_n	ACT_n	RAS_n	CAS_n /A15	WE_n /A14	BG0-BG1	BA0-BA1	A12/ BC_n	A13, A11	A10 /AP	A0-A6	Note
		PREV	CUR												
Read with Auto Precharge (BC4, on the Fly)	RDAS4	H	H	L	H	H	L	H	BG	BA	L	V	H	CA	
Read with Auto Precharge (BL8, on the Fly)	RDAS8	H	H	L	H	H	L	H	BG	BA	H	V	H	CA	
No Operation	NOP	H	H	L	H	H	H	H	V	V	V	V	V	V	
Device Deselected	DES	H	H	H	X	X	X	X	X	X	X	X	X	X	
Power-Down Entry	PDE	H	H	H	X	X	X	X	X	X	X	X	X	X	6
Power-Down Exit	PDX	L	H	H	X	X	X	X	X	X	X	X	X	X	6
ZQ calibration Long	ZQCL	H	H	L	H	H	H	L	V	V	V	V	H	V	

Notes:

1. All ST-DDR4 commands are defined by states of CS_n, ACT_n, RAS_n, CAS_n/A15, WE_n/A14 and CKE at the rising edge of the clock. The MSB of BG, BA, RA and CA are device density and configuration dependent. When ACT_n = H; pins RAS_n, CAS_n/A15, and WE_n/A14 are used as command pins RAS_n, CAS_n, and WE_n respectively. When ACT_n = L; pins RAS_n, CAS_n/A15, and WE_n/A14 are used as address pins A15 and A14 respectively.
2. RESET_n is Low enable command which will be used only for asynchronous reset so must be maintained HIGH during any function.
3. Bank Group addresses (BG) and Bank addresses (BA) determine which bank within a bank group to be operated upon. For MRS commands the BG and BA selects the specific Mode Register location.
4. “V” means a defined logic level and “X” means “Don’t Care”
5. Burst reads or writes cannot be terminated or interrupted and Fixed/on-the-Fly BL will be defined by MRS.

6. The Power Down Mode does not perform any refresh operation.
7. The state of ODT does not affect the states described in this table.
8. Controller guarantees self-refresh exit to be synchronous.
9. VREF(VREFCA) must be maintained during Self-refresh operation. The first Write Leveling Activity may occur after tXS time after exit from Self-refresh.
10. Refer to the CKE Truth Table for more detail with CKE transition.
11. The REFRESH command is used to execute the store all operation. See REFRESH Command (store all operation) on page 114.

Table 61 - Burst Length, Type and Order

Burst Length	Read / Write	Starting Column Address (A2, A1, A0)	Burst Type = Sequential (decimal) A3=0	Burst Type = Interleaved (decimal) A3=1	Notes
4	READ	0, V, V	0,1,2,3,T,T,T,T	Not Supported	1,2,3,4
		1, V, V	4,5,6,7,T,T,T,T	Not Supported	1,2,3,4
	WRITE	0, V, V	0,1,2,3,X,X,X,X	Not Supported	1,2,4,5
		1, V, V	4,5,6,7,X,X,X,X	Not Supported	1,2,4,5
8	READ	0, V, V	0,1,2,3,4,5,6,7	Not Supported	2,4
		1, V, V	Not Supported	Not Supported	2,4
	WRITE	V, V, V	0,1,2,3,4,5,6,7	Not Supported	2,4

Notes:

1. In case of burst length being fixed to 4 by MR0 setting, the internal write operation starts two clock cycles earlier than for the BL8 mode. This means that the starting point for tWR and tWTR will be pulled in by two clocks. In case of burst length being selected on-the-fly via A12/BC_n, the internal write operation starts at the same point in time like a burst of 8 write operation. This means that during on-the-fly control, the starting point for tWR and tWTR will not be pulled in by two clocks.
2. 0...7 bit number is value of CA[2:0] that causes this bit to be the first read during a burst.
3. T: Output driver for data and strobes are in high impedance.
4. V: A valid logic level (0 or 1), but respective buffer input ignores level on input pins. 5.
5. X : Don’t Care

12.1 DLL

The DLL must be enabled for normal operation and is required during power-up initialization and upon returning to normal operation after having the DLL disabled. During normal operation (DLL enabled with MR1[A0]) the DLL is automatically disabled when entering the SELF-REFRESH operation and is automatically re-enabled upon exit of the SELF-REFRESH operation. Any time the DLL is enabled and subsequently reset, tDLLK clock cycles must occur before a READ can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to

wait for synchronization to occur may result in a violation of the tDQSCK, tAON, or tAOF parameters.

During tDLLK, CKE must continuously be registered HIGH. The device does not require DLL for any WRITE operation.

12.1.1 DLL On/Off Switching Procedure

ST-DDR4 DLL-off mode is entered by setting MR1 bit A0 to 0; this will disable the DLL for subsequent operations until A0 bit is set back to 1.

12.1.2 Switch DLL to Off

To switch from DLL-on to DLL-off requires the frequency to be changed during self-refresh, as outlined in the following procedure:

1. Starting from the idle state (all banks pre-charged, all timings fulfilled.
2. Set MR1 bit A0 to 0 to disable the DLL.
3. Wait tMOD.
4. Enter self-refresh mode; wait until tCKSRE is satisfied.
5. Change frequency, following the guidelines in the Input Clock Frequency Change section.
6. Wait until a stable clock is available for at least tCKSRX at device inputs.
7. Starting with the SELF-REFRESH EXIT command, CKE must continuously be registered HIGH until all tMOD timings from any MRS command are satisfied.
8. Wait tXS_FAST, tXS_ABORT, or tXS, and then set mode registers with appropriate values (an update of CL, CWL, and WR may be necessary; a ZQCL command can also be issued after tXS_FAST).
9. tXS_FAST: ZQCL and MRS commands. For MRS commands, only CL and WR/RTP registers in MR0, the CWL register in MR2, and gear-down mode in MR3 may be accessed provided the device is not in Per Device Addressability mode. Access to other device mode registers must satisfy tXS timing.
10. tXS_ABORT: The controller can issue a valid command after a delay of tXS_ABORT. Upon exiting from self-refresh, the device requires a minimum of one extra REFRESH command before it is put back into self-refresh mode. This requirement remains the same regardless of the MRS bit setting for self-refresh abort.
11. tXS: ACT, PRE, PREA, REF, SRE, PDE, WR, WRS4, WRS8, WRA, WRAS4, WRAS8, RD, RDS4, RDS8, RDA, RDAS4, and RDAS8.
12. Wait for t_{MOD} to complete.
13. The device is ready for the next command.

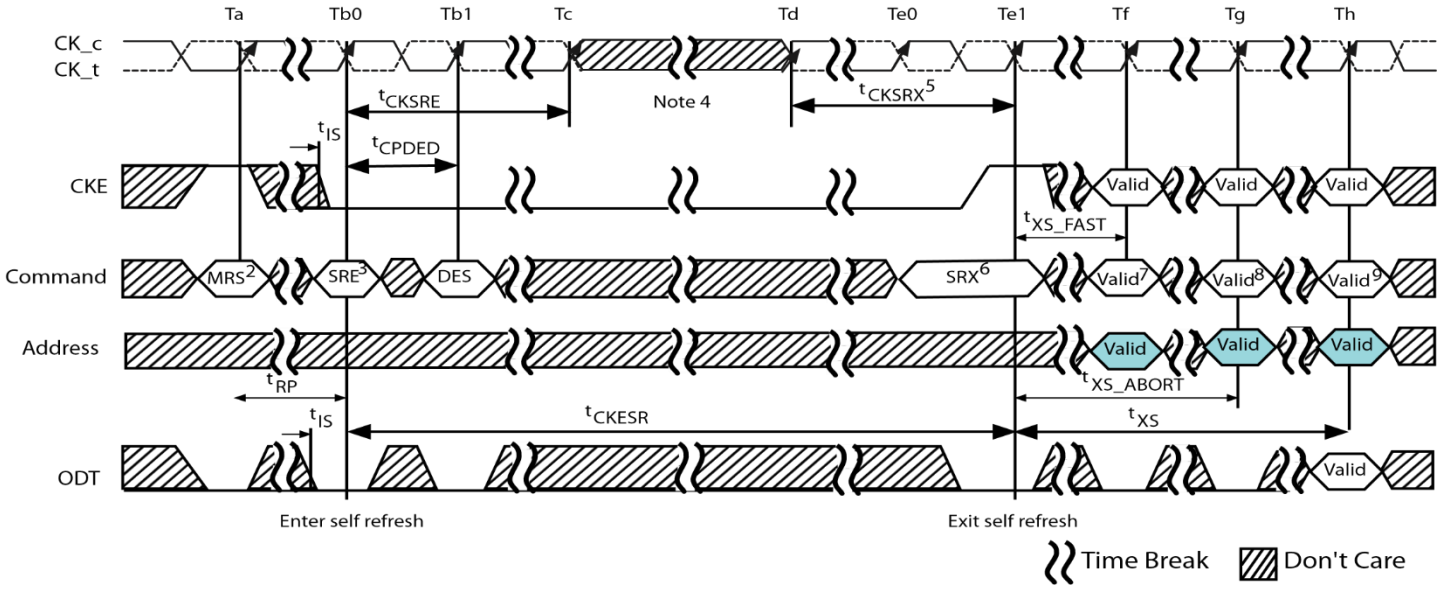

Figure 16 - DLL Off Sequence

Notes:

1. Starting in the idle state.
2. Disable DLL by setting MR1 bit A0 to 0.
3. Enter SR.
4. Change Frequency.
5. Clock must be stable t_{CKSRX}.
6. Exit SR.
7. Update mode registers allowed with DLL-off settings met.
8. $R_{TT(Park)}$ is the only ODT mode supported
9. $R_{TT(NOM)}$ and $R_{TT(WR)}$ is not supported

12.1.3 DLL Off Mode

DLL-off mode is entered by setting MR1 bit A0 to 0; this will disable the DLL for subsequent operations until A0 bit is set back to 1. The MR1 A0 bit for DLL control can be switched either during initialization or later. Refer to, section “22.1 Input Clock Frequency Change “

The DLL-off Mode operations listed below are an optional feature. The maximum clock frequency for DLL-off Mode is specified by the parameter tCKDLL(OFF).

Due to latency counter and timing restrictions, only one value of CAS Latency (CL) in MR0 and CAS Write Latency (CWL) in MR2 are supported. The DLL-off mode is only required to support setting of both CL=10 and CWL=9.

DLL-off mode will affect the Read data Clock to Data Strobe relationship (tDQSCK), but not the Data Strobe to Data relationship (tDQSQ, tQH). Special attention is needed to line up Read data to controller time domain.

Comparing with DLL-on mode, where tDQSCK starts from the rising clock edge (CL) cycles after the Read command, the DLL-off mode tDQSCK starts (CL - 1) cycles after the read command. Another difference is that tDQSCK may not be small compared to tCK (it might even be larger than tCK) and the difference between tDQSCKmin and tDQSCKmax is significantly larger than in DLL-on mode. tDQSCK(DLL_off) values are vendor specific.

The timing relations on DLL-off mode READ operation are shown in the following Timing Diagram (CL=10, BL=8):

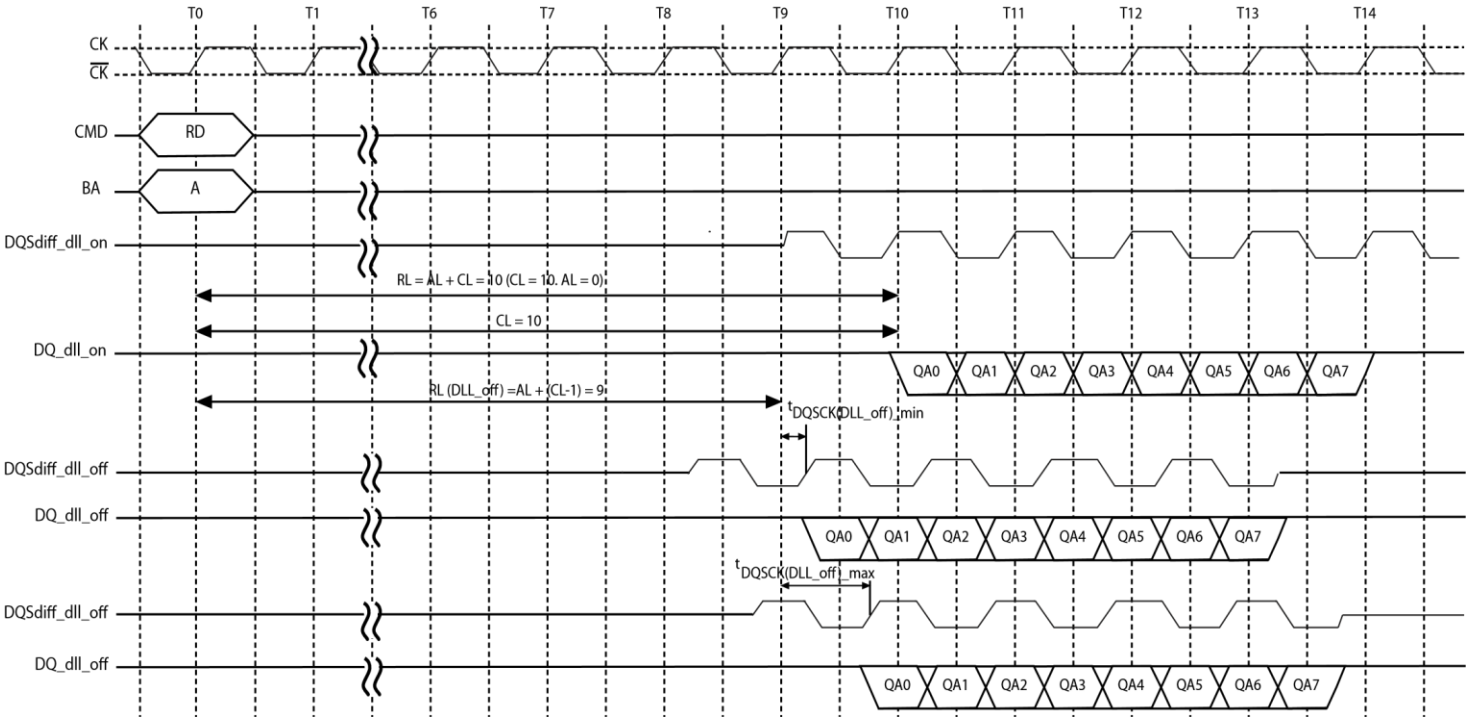

Figure 17 - Read Operation in DLL Off Mode

12.1.4 Switch DLL to On

To switch from DLL-off to DLL-on (with required frequency change) during self-refresh:

1. Starting from the idle state (all banks pre-charged, all timings fulfilled).
2. Enter self-refresh mode; wait until tCKSRE is satisfied.
3. Change frequency (following the guidelines in the Input Clock Frequency Change section).
4. Wait until a stable clock is available for at least tCKSRX at device inputs.
5. Starting with the SELF-REFRESH EXIT command, CKE must continuously be registered HIGH until tDLLK timing from the subsequent DLL RESET command is satisfied.

6. Wait tXS or tXS_ABORT, depending on bit A9 in MR4, then set MR1 bit A0 to 1 to enable the DLL.
7. Wait tMRD, then set MR1 bit A8 to 1 to start DLL reset.
8. Wait tMRD, then set mode registers with appropriate values; an update of CL, CWL, and WR may be necessary. After tMOD is satisfied from any proceeding MRS command, a ZQCL command can also be issued during or after tDLLK.
9. Wait for tMOD to complete. Remember to wait tDLLK after DLL RESET before applying any command requiring a locked DLL. In addition, wait for tZQoper in case a ZQCL command was issued.
   The device is ready for the next command.

12.2 Input Clock Frequency Change

After the device is initialized, it requires the clock to be stable during almost all states of normal operation. This means that after the clock frequency has been set and is in the stable state, the clock period is not allowed to deviate except for what is allowed by the clock jitter and spread spectrum clocking (SSC) specifications. The input clock frequency can be changed from one stable clock rate to another stable clock rate in two modes:

1. Self-refresh mode and
2. Precharge Power-down mode.

Outside of these modes, it is illegal to change the clock frequency.

For condition (1), after the device has been successfully placed in self-refresh mode and tCKSRE has been satisfied, the state of the clock becomes a “Don’t Care.” Following a “Don’t Care,” changing the clock frequency is permissible, provided the new clock frequency is stable prior to tCKSRX. When entering and exiting self-refresh mode for the sole purpose of changing the clock frequency, the self-refresh entry and exit specifications must still be met as outlined in “SELF-REFRESH ” section.
For the new clock frequency, additional MRS commands to MR0, MR2, MR3, MR4, and MR6 may need to be issued to program appropriate CL, CWL, gear-down mode, READ and WRITE preamble, and tCCD_L values.

The device input clock frequency can change only within the minimum and maximum operating frequency specified for the particular speed grade. Any frequency change below the minimum operating frequency would require the use of DLL-on mode to DLL-off mode transition sequence (DLL On/Off Switching Procedure on page 90).

The input clock frequency is allowed to change only within the minimum and maximum operating frequency specified for the particular speed grade. During the input clock frequency change, CKE must be held at stable LOW levels. Once the input clock frequency is changed, stable new clocks must be provided to the device, tCKSRX before Precharge Power-down may be exited; after Precharge Powerdown is exited and tXP has expired, tDLLK MRS command

followed by DLL reset must be issued. Depending on the new clock frequency, additional MRS commands may need to be issued to appropriately set the WR/RTP, CL, and CWL with CKE continuously registered high. During DLL re-lock period, CKE must remain HIGH. After the DLL lock time, the device is ready to operate with new clock frequency. This procedure is shown in "Figure 18 - Frequency Change During PRECHARGE Power Down" below.

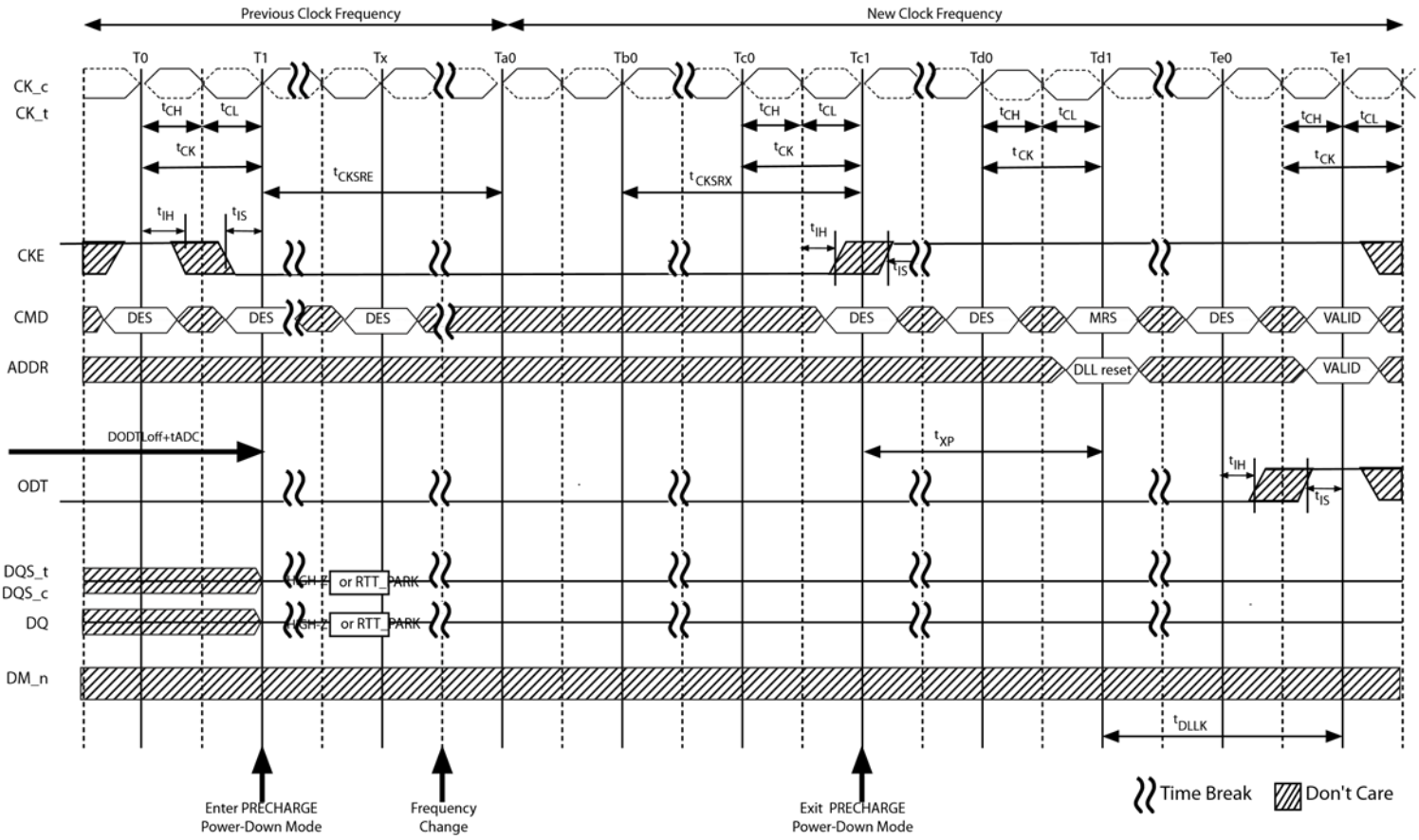

Figure 18 - Frequency Change During PRECHARGE Power Down

Notes:

1. tCKSRE and tCKSRX are Self-Refresh mode specification but the value they represent are applicable here.
2. If $R_{TT(PARK)}$ is disabled and ODT input buffer is not deactivated.
3. $R_{TT(PARK)}$ is the only ODT mode supported.
4. $R_{TT(NOM)}$ and $R_{TT(WR)}$ are not supported.
5. The ODT pin in a "don't care"

12.3 Write Leveling

For better signal integrity, DDR4 memory modules use fly-by topology for the commands, addresses, control signals, and clocks. Fly-by topology has benefits from the reduced number of stubs and their length, but it also causes flight-time skew between clock and strobe at every ST-DDR4 device on the DIMM. This makes it difficult for the controller to maintain tDQSS, tDSS, and tDSH specifications. Therefore, the device supports a write-leveling feature to allow the controller to compensate for skew. This feature may not be required under some system conditions, provided the host can maintain the tDQSS, tDSS, and tDSH specifications.

The memory controller can use the write-leveling feature and feedback from the device to adjust the DQS (DQS_t, DQS_c) to CK (CK_t, CK_c) relationship. The memory controller involved in the leveling must have an adjustable delay setting on DQS to align the rising edge of DQS with that of the clock at the device pin. The device asynchronously feeds back CK, sampled with the rising edge of DQS, through the DQ bus. The controller repeatedly delays DQS until a transition from 0 to 1 is detected. The DQS delay established though this exercise would ensure the tDQSS specification. Besides tDQSS, tDSS and tDSH specifications also need to be fulfilled. One way to achieve this is to combine the actual tDQSS in the application with an appropriate duty cycle and jitter on the DQS signals. Depending on the actual tDQSS in the application, the actual values for tDQSL and tDQSH may have to be better than the absolute limits provided in the AC Timing Parameters section in order to satisfy tDSS and tDSH specifications. A conceptual timing of this scheme is shown below.

12.4 Settings for Write Leveling and Termination

The device enters into write-leveling mode if A7 in MR1 is HIGH. When leveling is finished, the device exits write-leveling mode if A7 in MR1 is LOW. Note that in write-leveling mode, only DQS terminations are activated and deactivated via the ODT pin, unlike normal operation See “Table 62 - MR Settings for Leveling Procedures” below.

Table 62 - MR Settings for Leveling Procedures

Function	MR1	Enable	Disable
Write leveling enable	A7	1	0
Output buffer mode (Q off)	A12	0	1

12.5 Write Leveling Procedure Description

The Memory controller initiates Leveling mode of all ST-DDR4 devices by setting bit A7 of MR1 to 1. When entering write leveling mode, the DQ pins are in an undefined driving mode. During write leveling mode, only DESELECT commands are allowed, as well as an MRS command to change Qoff bit (MR1[A12]) and an MRS command to exit write leveling (MR1[A7]). Upon exiting write leveling mode, the MRS command performing the exit (MR1[A7]=0) may also change MR1 bits of A12-A8 ,A2-A1. Since the controller levels one rank at a time, the output of other ranks must be disabled by setting MR1 bit A12 to 1.

The Controller may drive DQS_t low and DQS_c high after a delay of tWLDQSEN, at which time the DRAM has applied on-die termination on these signals. After tDQSL and tWLMRD, the controller provides a single DQS_t, DQS_c edge which is used by the device to sample CK_t - CK_c driven from controller. tWLMRD(max) timing is controller dependent.

DRAM samples CK_t - CK_c status with rising edge of DQS_t - DQS_c and provides feedback on all the DQ bits asynchronously after tWLO timing. There is a DQ output uncertainty of tWLOE defined to allow mismatch on DQ bits. The tWLOE period is defined from the transition of the earliest DQ bit to the corresponding transition of the latest DQ bit. There are no read strobes (DQS_t/DQS_c) needed for these DQs. Controller samples incoming DQs and decides to increment or decrement DQS_t - DQS_c delay setting and launches the next DQS_t/DQS_c pulse after some time, which is controller dependent. Once a 0 to 1 transition is detected, the controller locks the DQS_t - DQS_c delay setting and write leveling is achieved for the device. "Figure 19 - Timing details of the Write Leveling Sequence" illustrates the timing diagram and parameters for the overall Write Leveling procedure.

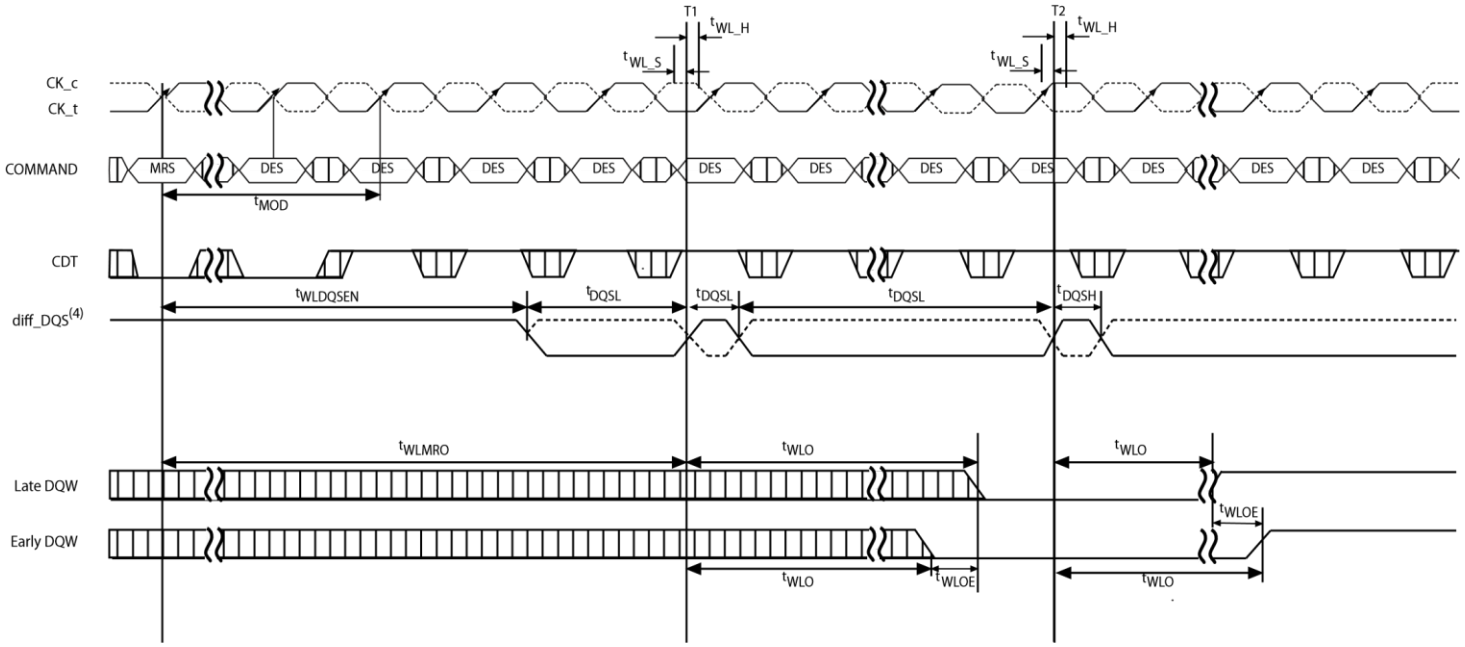

Figure 19 - Timing details of the Write Leveling Sequence

Notes:

1. DDR4 SDRAM drives leveling feedback on all DQs
2. MRS : Load MR1 to enter write leveling mode
3. DES : Deslect
4. diff_DQS is the differential data strobe (DQS_t-DQS_c). Timing reference points are the zero crossrings. DQS is shown with solid line, DQS_c is shown with dotted line
5. CK_t/CK_c : CK is shown with solid dark line, where as CK_c is drawn with dotted line.

6. DQS_t, DQS_c needs to fulfill minimum pulse width requirements tDQSH(min) and tDQSL(min) as defined for regular Writes; the max pulse width is system dependent.

12.6 Write Leveling Mode Exit

Write-leveling mode should be exited as follows:

1. After the last rising strobe edge (see ~T0), stop driving the strobe signals (see ~Tc0). Note that from this point on, DQ pins are in undefined driving mode and will remain undefined, until tMOD after the respective MR command (Te1).
2. Drive ODT pin LOW (tIS must be satisfied) and continue registering LOW (see Tb0).
3. After R_{TT} is switched off, disable write-leveling mode via the MRS command (see Tc2).
4. After tMOD is satisfied (Te1), any valid command can be registered. (MR commands can be issued after tMRD [Td1]).

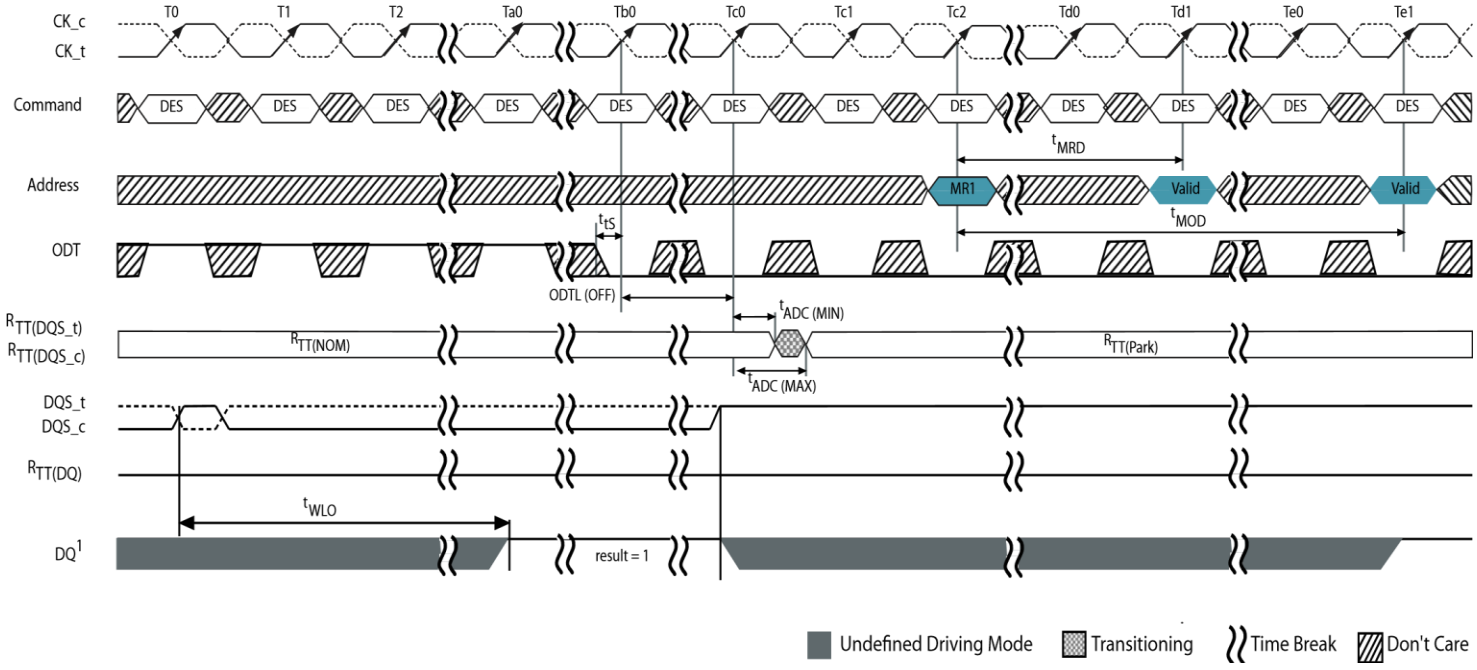

Figure 20 - Write Leveling Exit

Notes:

1. The DQ result = 1 between Ta0 and Tc0 is a result of the DQS signals capturing CK_t HIGH just after the T0 state.
2. See previous figure for specific tWLO timing.

12.7 Per Device Addressability (PDA)

DDR4 allows programmability of a single, specific device on a rank. As an example, this feature can be used to program different values on each device on a given rank. Because Per Device Addressability (PDA) mode may be used to program optimal V_{REF} for each device, the data setup for first DQ0 transfer or the hold time for the last DQ0 transfer cannot be guaranteed. The device may sample DQ0 on either the first falling or second rising DQS transfer edge. This supports a common implementation between BC4 and BL8 modes on the device. The ST-DDR4 controller is required to drive DQ0 to a stable LOW or HIGH state during the length of the data transfer for BC4 and BL8 cases.

1. Before entering PDA mode, write leveling is required.
   - BL8 or BC4 may be used.
2. Before entering PDA mode, the following MR settings are possible:
   - $R_{TT(PARK)}$ MR5 A[8:6] = Enable
3. Enable PDA mode using MR3[A4] = 1. (The default programed value of MR3[A4] = 0.)
4. In PDA mode, all MRS commands are qualified with DQ0. The device captures DQ0 by using DQS signals. If the value on DQ0 is LOW, the device executes the MRS command. If the value on DQ0 is HIGH, the device ignores the MRS command. The controller can choose to drive all the DQ bits.
5. Program the desired ST-DDR4 device and mode registers using the MRS command and DQ0.
6. In PDA mode, only MRS commands are allowed.
7. The MODE REGISTER SET command cycle time in PDA mode, CWL + BL/2 - 0.5tCK + tMRD_PDA, is required to complete the WRITE operation to the mode register and is the minimum time required between two MRS commands.
8. Remove the device from PDA mode by setting MR3[A4] = 0. (This command requires DQ0 = 0.)

Note: Removing the device from PDA mode will require programming the entire MR3 when the MRS command is issued. This may impact some PDA values programmed within a rank as the EXIT command is sent to the rank. To avoid such a case, the PDA enable/disable control bit is located in a mode register that does not have any PDA mode controls.

In PDA mode, the device captures DQ0 using DQS signals the same as in a normal WRITE operation.

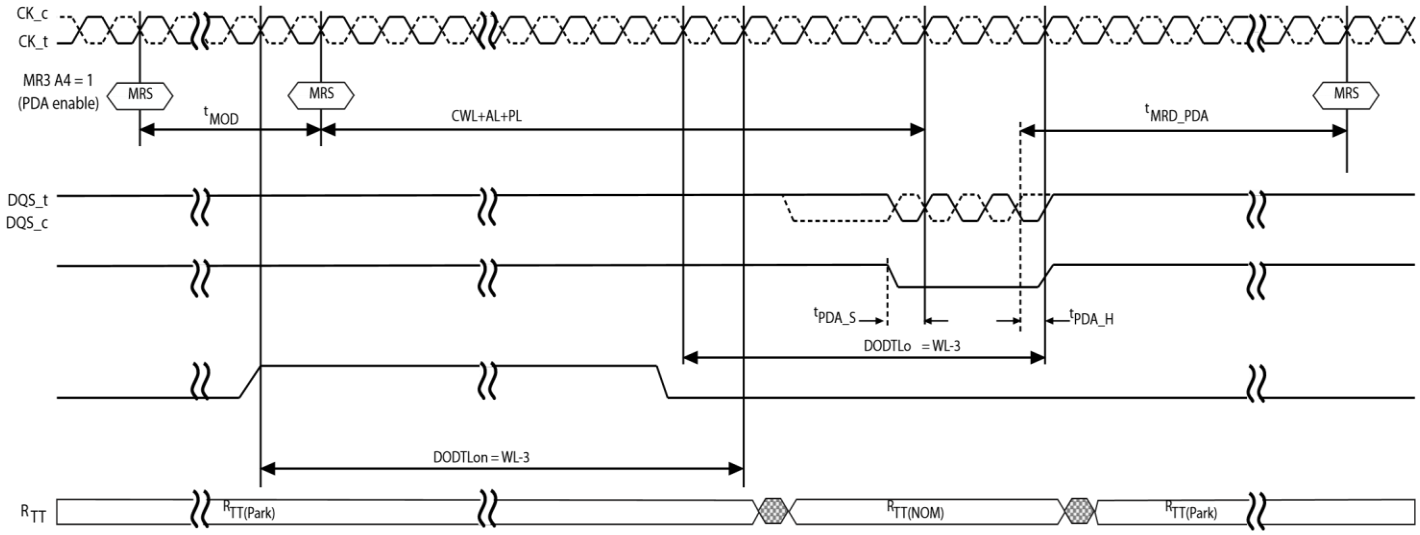

Figure 21 - PDA Operation Enabled, BL8

Notes:

1. $R_{TT(PARK)}$ = Enable; WRITE preamble set =2tCK; and DLL = on.

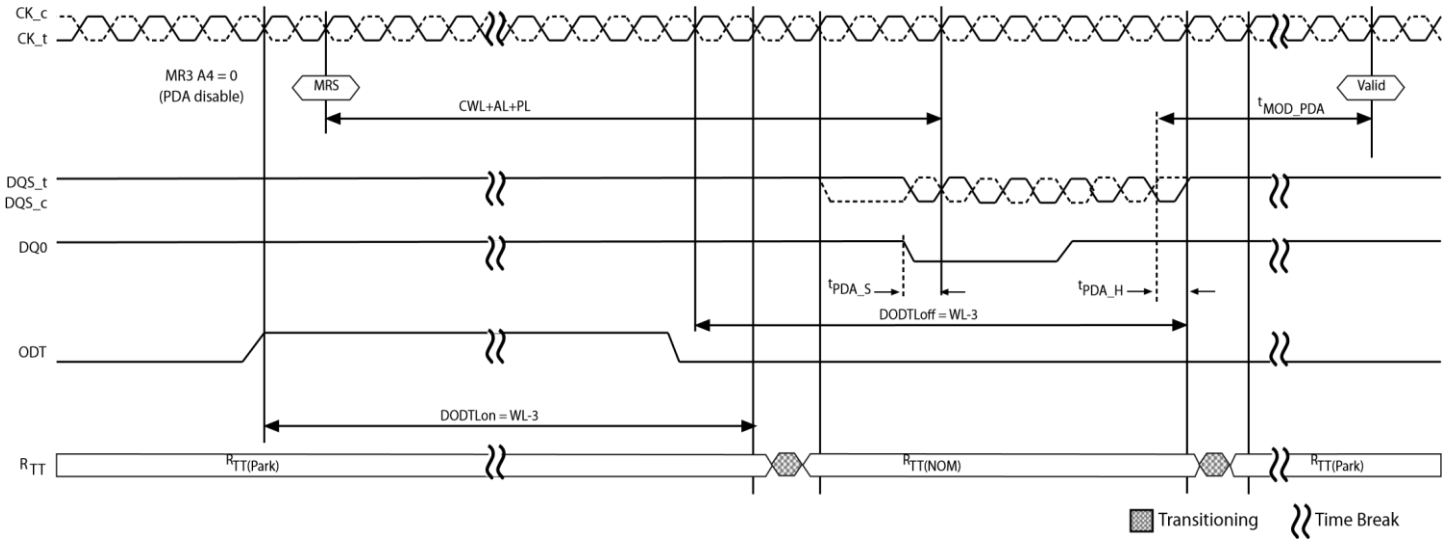

Figure 22 - MRS PDA Exit

Notes:

1. $R_{TT(PARK)}$ = Enable; WRITE preamble set =2tCK; and DLL = on.

12.8 VREFDQ Calibration

The VREFDQ level, which is used by the device DQ input receivers, is internally generated. The device's VREFDQ does not have a default value upon power-up and must be set to the desired value, usually via

VREFDQ calibration mode. If PDA or PPR modes are used prior to VREFDQ calibration, VREFDQ should initially be set at the midpoint between the VDD,max, and the LOW as determined by the driver and ODT termination selected with wide voltage swing on the input levels and setup and hold times of approximately 0.75UI. The memory controller is responsible for VREFDQ calibration to determine the best internal VREFDQ level.

The VREFDQ calibration is enabled/disabled via MR6[A7], MR6[A6] selects Range 1 (60% to 92.5% of VDDQ) or Range 2 (45% to 77.5% of VDDQ), and an MRS protocol using MR6[A5:A0] to adjust the VREFDQ level up and down. MR6[A6:A0] bits can be altered using the MRS command if MR6[A7] is disabled. The ST-DDR4 controller will likely use a series of writes and reads in conjunction with VREFDQ adjustments to obtain the best VREFDQ, which in turn optimizes the data eye.

The internal VREFDQ specification parameters are voltage range, step size, VREF step time, VREF full step time, and VREF valid level. The voltage operating range specifies the minimum required VREF setting range for ST-DDR4 devices. The minimum range is defined by VREFDQ,min and VREFDQ,max. As noted, a calibration sequence, determined by the ST-DDR4 controller, should be performed to adjust VREFDQ and optimize the timing and voltage margin of the device data input receivers. The internal VREFDQ voltage value may not be exactly within the voltage range setting coupled with the VREF set tolerance; the device must be calibrated to the correct internal VREFDQ voltage.

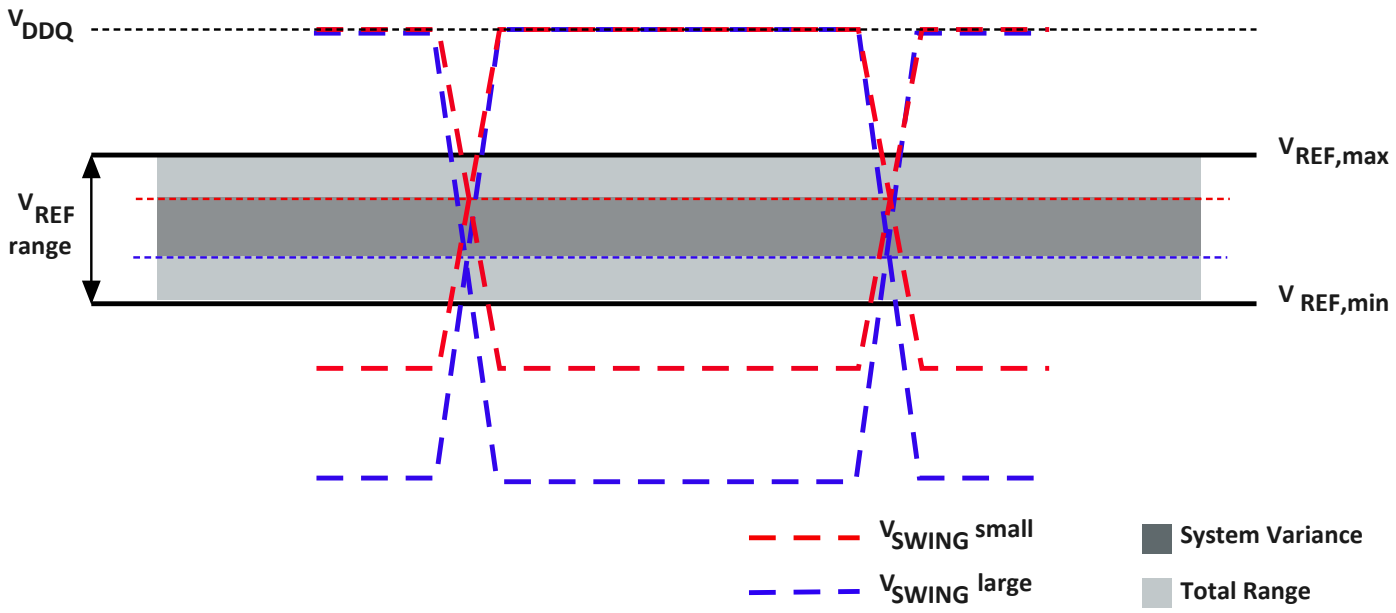

Figure 23 - VREFDQ Voltage Range

12.9 VREFDQ Step Size

The VREF step size is defined as the step size between adjacent steps. VREF step size ranges from 0.5% VDDQ to 0.8% VDDQ. However, for a given design, the device has one value for VREF step size that falls within the range.

The VREF set tolerance is the variation in the VREF voltage from the ideal setting. This accounts for accumulated error over multiple steps. There are two ranges for VREF set tolerance uncertainty. The range of VREF set tolerance uncertainty is a function of number of steps n. The VREF set tolerance is measured with respect to the ideal line, which is based on the MIN

and MAX VREF value endpoints for a specified range. The internal V_{REFDQ} voltage value may not be exactly within the voltage range setting coupled with the VREF set tolerance; the device must be calibrated to the correct internal V_{REFDQ} voltage.

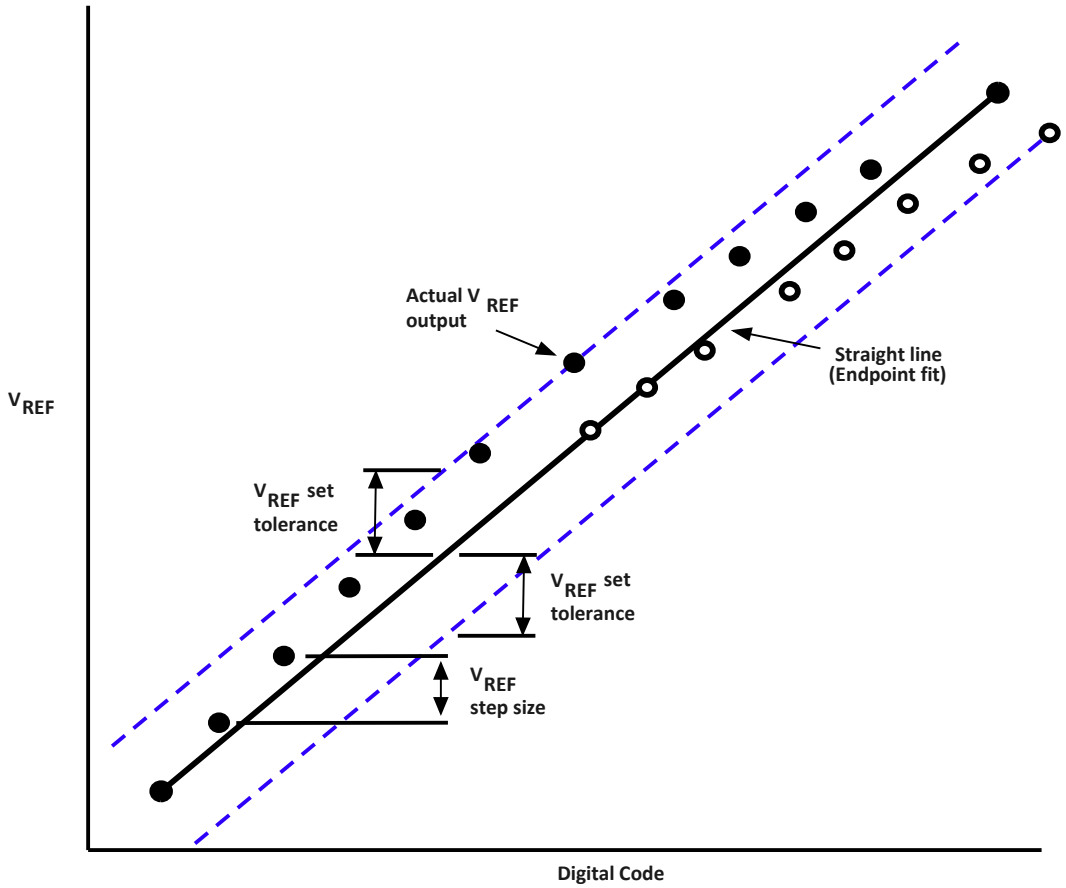

Figure 24 - Example of VREF Set Tolerance and Step Size

Notes:

1. Maximum case shown

12.10 VREFDQ Increment and Decrement Timing

The VREF increment/decrement step times are defined by VREF,time. VREF,time is defined from t0 to t1, where t1 is referenced to the VREF voltage at the final DC level within the VREF valid tolerance (VREF,val_tol). The VREF valid level is defined by VREF,val tolerance to qualify the step time t1. This parameter is used to insure an adequate RC time constant behavior of the voltage level change after any VREF increment/decrement adjustment.

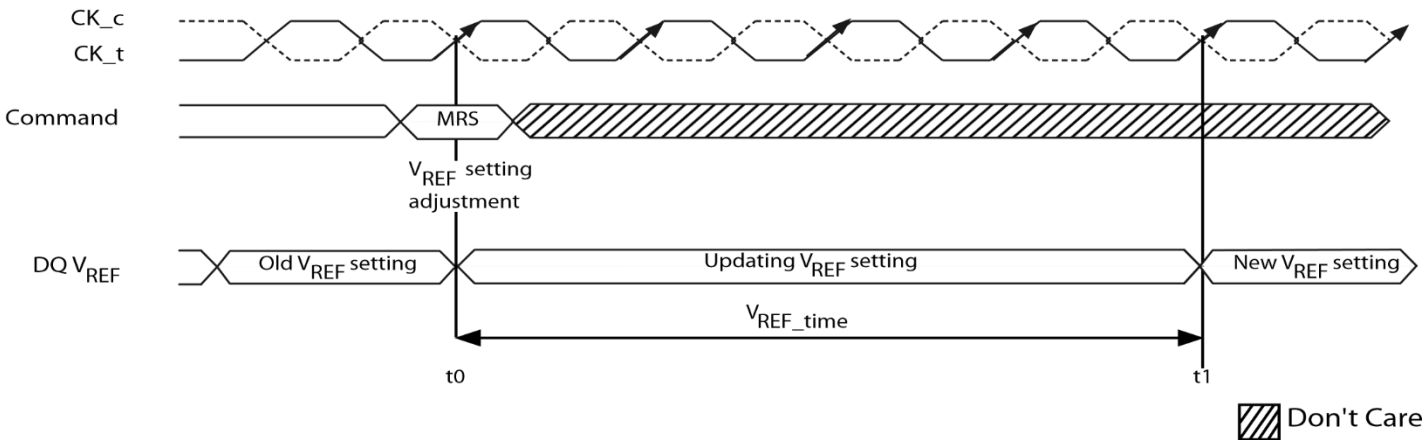

Figure 25 - V_{REFDQ} Timing Diagram for $V_{REF,time}$ Parameter

Notes:

1. t0 is referenced to the MRS command clock.
2. t1 is referenced to $V_{REF,tol}$.

V_{REFDQ} calibration mode is entered via an MRS command, setting MR6[A7] to 1 (0 disables V_{REFDQ} calibration mode) and setting MR6[A6] to either 0 or 1 to select the desired range (MR6[A5:A0] are "Don't Care"). After V_{REFDQ} calibration mode has been entered, V_{REFDQ} calibration mode legal commands may be issued once $t_{VREFDQE}$ has been satisfied. Legal commands for V_{REFDQ} calibration mode are ACT, WR, WRA, RD, RDA, PRE, DES, and MRS to set V_{REFDQ} values, and MRS to exit V_{REFDQ} calibration mode. Also, after V_{REFDQ} calibration mode has been entered, "dummy" WRITE commands are allowed prior to adjusting the V_{REFDQ} value the first time V_{REFDQ} calibration is performed after initialization. Setting V_{REFDQ} values requires MR6[A7] be set to 1 and MR6[A6] be unchanged from the initial range selection; MR6[A5:A0] may be set to the desired V_{REFDQ} values. If MR6[A7] is set to 0, MR6[A6:A0] are not written. $V_{REF,time-short}$ or $V_{REF,time-long}$ must be satisfied after each MR6 command to set V_{REFDQ} value before the internal V_{REFDQ} value is valid.

If PDA mode is used in conjunction with V_{REFDQ} calibration, the PDA mode requirement that only MRS commands are allowed while PDA mode is enabled is not waived. That is, the only V_{REFDQ} calibration mode legal commands noted above that may be used are the MRS commands: MRS to set V_{REFDQ} values and MRS to exit V_{REFDQ} calibration mode.

The last MR6[A6:A0] setting written to MR6 prior to exiting V_{REFDQ} calibration mode is the range and value used for the internal V_{REFDQ} setting. Existing V_{REFDQ} calibration mode is allowed when the device is in idle state. After the MRS command to exit V_{REFDQ} calibration mode has been issued, DES must be issued until $t_{VREFDQX}$ has been satisfied where any legal command may then be issued. V_{REFDQ} setting should be updated if the die temperature changes too much from the calibration temperature.

12.10.1 Range 1 Calibration

The following is a typical script when applying the above rules for V_{REFDQ} calibration routine when performing V_{REFDQ} calibration in Range 1:

1. MR6[A7:A6]10 [A5:A0]XXXXXXX.
   - Subsequent legal commands while in V_{REFDQ} calibration mode: ACT, WR, WRA, RD, RDA, PRE, DES, and MRS (to set V_{REFDQ} values and exit V_{REFDQ} calibration mode).
   - All subsequent V_{REFDQ} calibration MR setting commands are MR6[A7:A6]10[A5:A0]VVVVVV.
   - "VVVVVV" are desired settings for V_{REFDQ}.
2. Issue ACT/WR/RD looking for pass/fail to determine V_{CENT} (midpoint) as needed.

To exit V_{REFDQ} calibration, the last two V_{REFDQ} calibration MR commands are:

1. MR6[A7:A6]10 [A5:A0]VVVVVV* [where VVVVVV* = desired value for V_{REFDQ}.]
2. MR6[A7]0 [A6:A0]XXXXXXX [to exit V_{REFDQ} calibration mode.]

12.10.2 Range 2 Calibration

The following is a typical script when applying the above rules for V_{REFDQ} calibration routine when performing V_{REFDQ} calibration in Range 2:

1. MR6[A7:A6]11 [A5:A0]XXXXXXX.
2. Subsequent legal commands while in V_{REFDQ} calibration mode: ACT, WR, WRA, RD, RDA, PRE, DES, and MRS (to set V_{REFDQ} values and exit V_{REFDQ} calibration mode).
3. All subsequent V_{REFDQ} calibration MR setting commands are MR6[A7:A6]11[A5:A0]VVVVVV.
4. "VVVVVV" are desired settings for V_{REFDQ}.
5. Issue ACT/WR/RD looking for pass/fail to determine V_{CENT} (midpoint) as needed.

To exit V_{REFDQ} calibration, the last two V_{REFDQ} calibration MR commands are:

1. MR6[A7:A6]11 [A5:A0]VVVVVV* where VVVVVV* = desired value for V_{REFDQ}.
2. MR6[A7]0 [A6:A0]XXXXXXX to exit VREFDQ calibration mode.

Note:

1. Range may only be set or changed when entering V_{REFDQ} calibration mode; changing range while in or exiting V_{REFDQ} calibration mode is illegal.

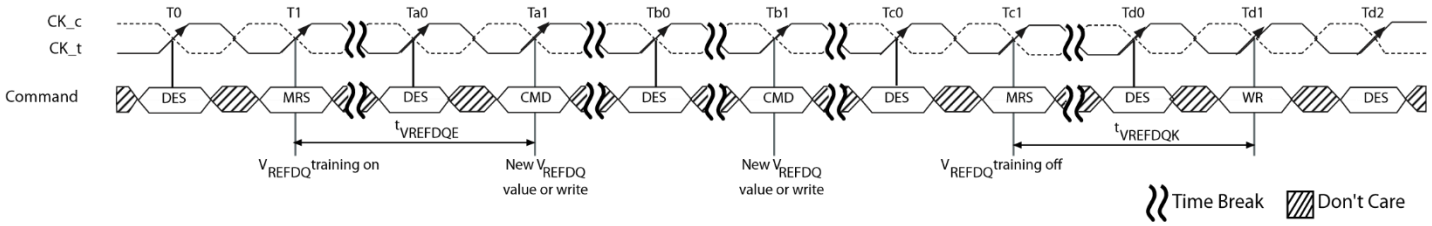

Figure 26 - Training Mode Entry and Exit Timing Diagram

Notes:

1. New V_{REFDQ} values are not allowed with an MRS command during calibration mode entry.
2. Depending on the step size of the latest programmed V_{REF} value, V_{REF} must be satisfied before disabling V_{REFDQ} training mode.

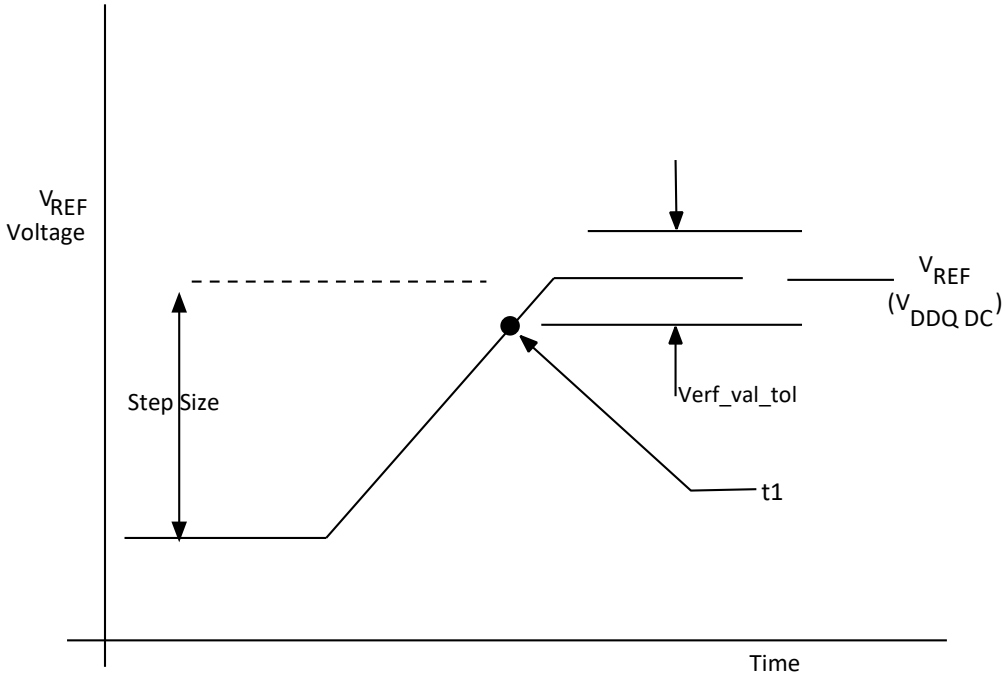

Figure 27 - VREF Single Step Size Increment Case

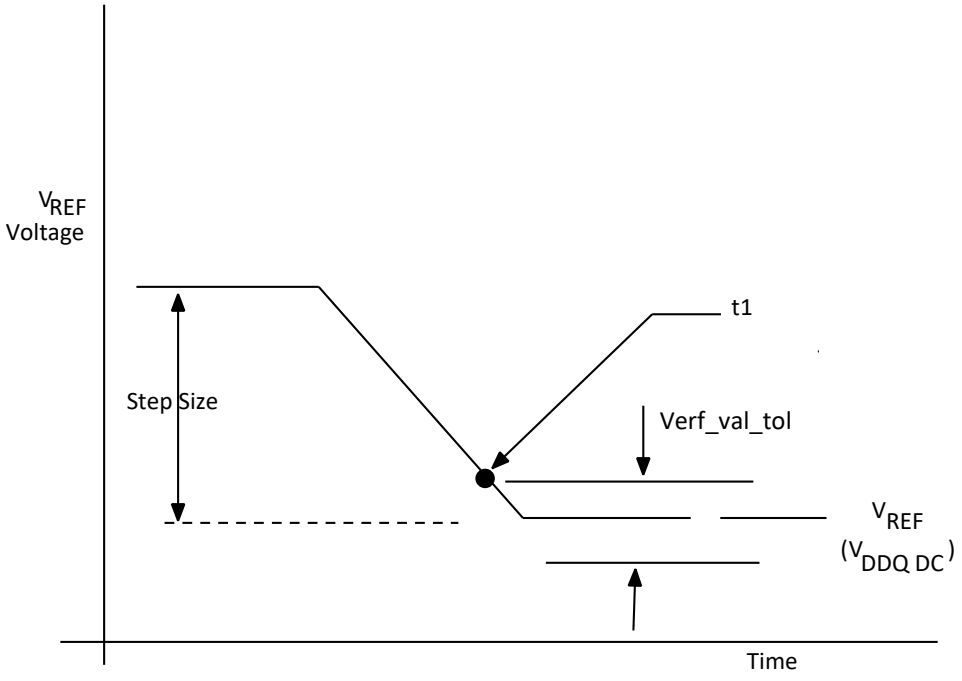

Figure 28 - VREF Single Step Decrement Case

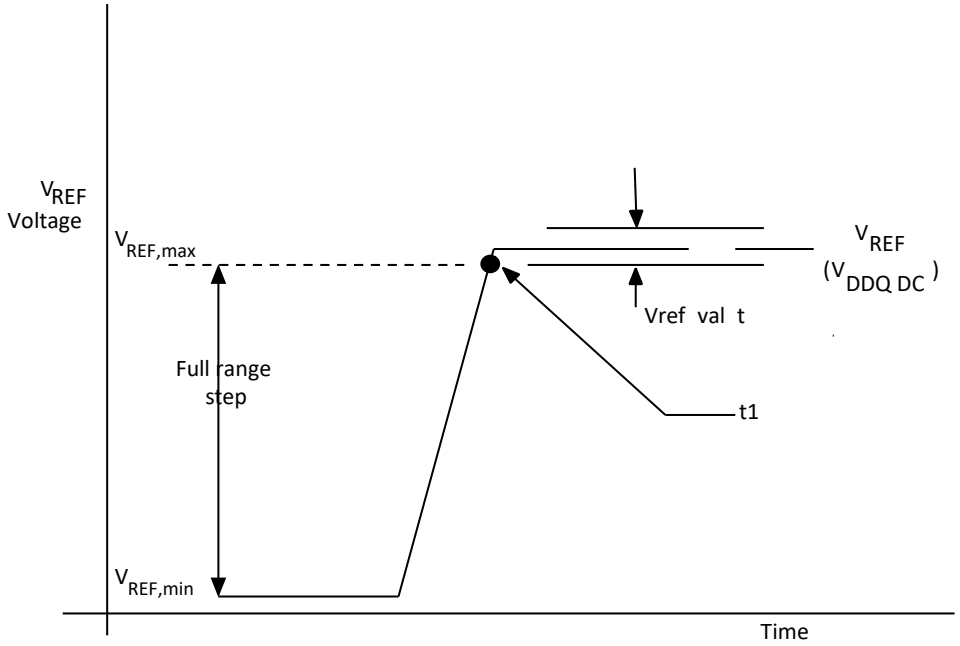

Figure 29 - VREF Full Step: $V_{REF,min}$ to $V_{REF,max}$

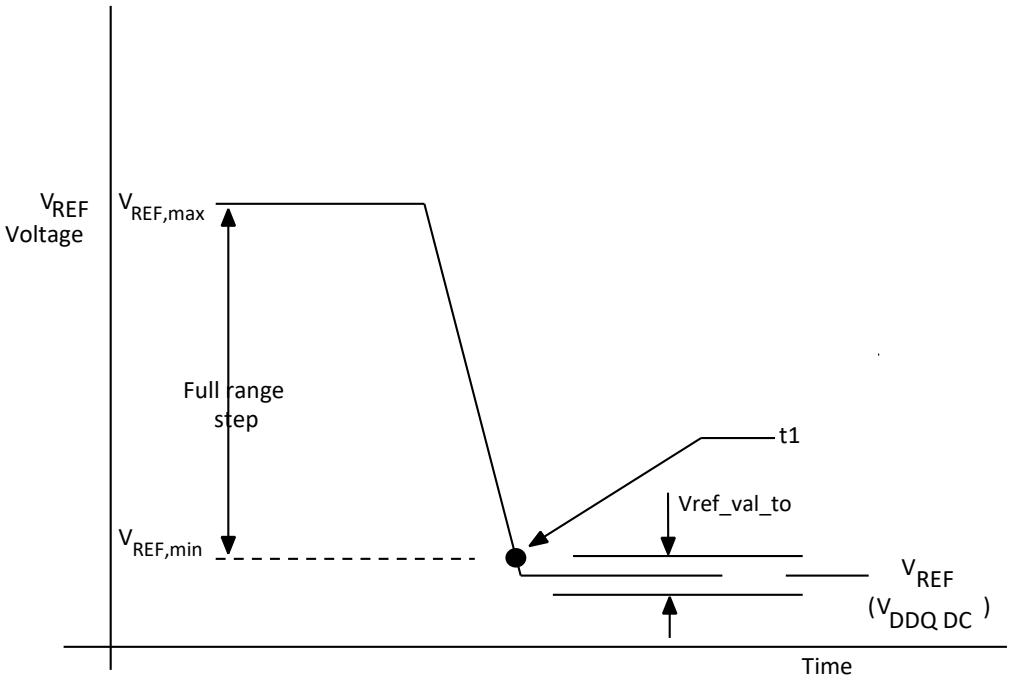

Figure 30 - VREF Single Step Decrement Case

12.11 VREFDQ Target Settings

The VREFDQ initial settings are largely dependent on the ODT termination settings. The table below shows all the possible initial settings available for VREFDQ training; it is unlikely the lower ODT settings would be used in most cases

Table 63 - V_{REFDQ} Target Settings (V_{DDQ} = 1.2V)

RON	ODT	VX – VIN LOW (mV)	V_{REFDQ} (mV)	V_{REFDQ} (%VDDQ)
	34 ohms	600	900	75%
34 Ohms	40 ohms	550	875	73%
	48 ohms	500	850	71%
	60 ohms	435	815	68%
	80 ohms	360	780	65%
	120 ohms	265	732	61%
	240 ohms	150	675	56%
48 Ohms	34 ohms	700	950	79%
	40 ohms	655	925	77%
	48 ohms	600	900	75%
	60 ohms	535	865	72%
	80 ohms	450	825	69%
	120 ohms	345	770	64%
	240 ohms	200	700	58%

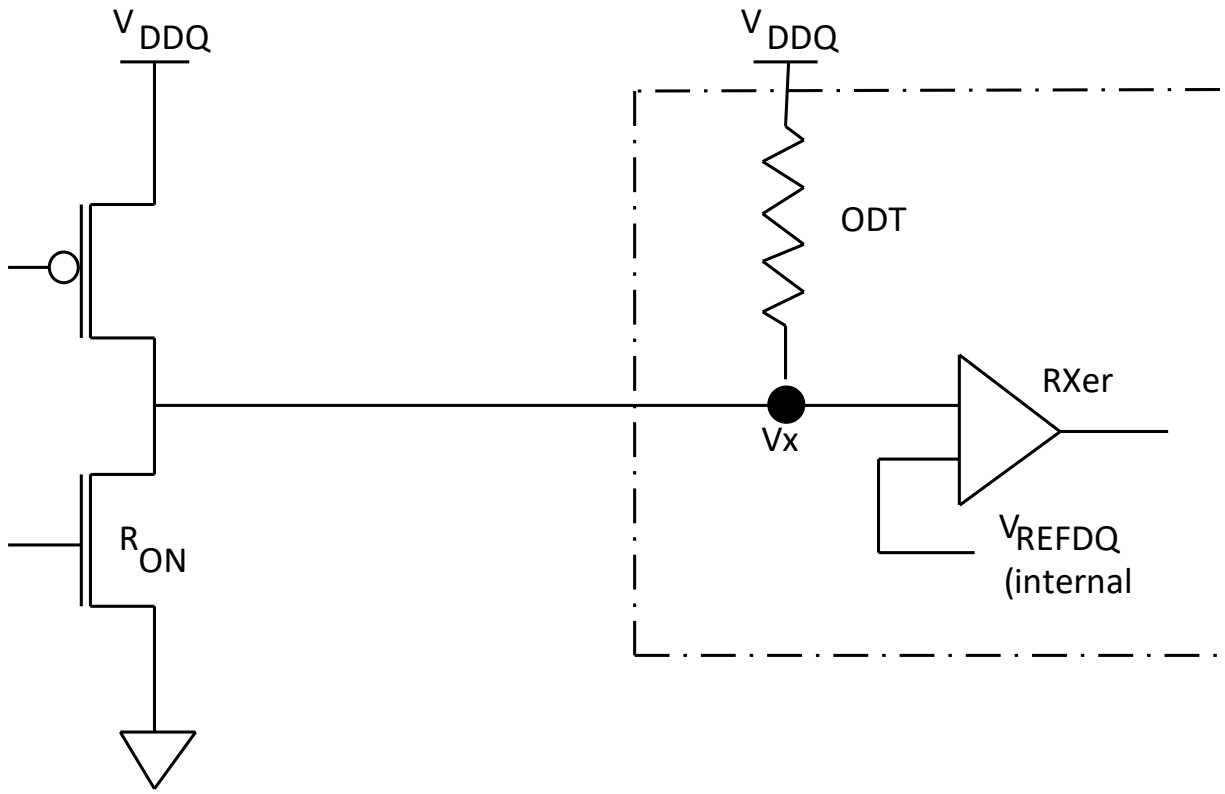

Figure 31 - VREFDQ Equivalent Circuit

12.12 Connectivity Test Mode

Connectivity Test (CT) Mode is similar to boundary scan testing but is designed to significantly speed up the testing of electrical continuity of pin interconnections between the device and the memory controller on the PC boards. The device is designed to work seamlessly with any boundary scan mechanism.

Contrary to other conventional shift-register-based test modes, where test patterns are shifted in and out of the memory devices serially during each clock, the CT mode allows test patterns to be entered on the test input pins in parallel and the test results to be extracted from the test output pins of the device in parallel. These two functions are also performed at the same time, significantly increasing the speed of the connectivity check. When placed in CT mode, the device appears as an asynchronous device to the external controlling agent. After the input test pattern is applied, the connectivity test results are available for extraction in parallel at the test output pins after a fixed propagation delay time.
Note: A reset of the device is required after exiting CT mode see (Figure 4 - VREFCA Voltage Range).

Only digital pins can be tested using the CT mode. For the purposes of a connectivity check, all the pins used for digital logic in the device are classified as one of the following types:

- **Test enable (TEN)**: When asserted HIGH, this pin causes the device to enter CT mode. In CT mode, the normal memory function inside the device is bypassed and the I/O pins appear as a set of test input and output pins to the external controlling agent. Additionally, the device will set the internal V_{REFDQ} to $V_{DDQ} \times 0.5$ during CT mode (this is the only time the device takes direct control over setting the internal V_{REFDQ}). The TEN pin is dedicated to the connectivity check function and will not be used during normal device operation.
- **Chip select (CS_n)**: When asserted LOW, this pin enables the test output pins in the device. When de-asserted, these output pins will be High-Z. The CS_n pin in the device serves as the CS_n pin in CT mode.
- **Test input**: A group of pins used during normal device operation designated as test input pins. These pins are used to enter the test pattern in CT mode.
- **Test output**: A group of pins used during normal device operation designated as test output pins. These pins are used for extraction of the connectivity test results in CT mode.
- **RESET_n**: This pin must be fixed high level during CT mode, as in normal function.

Table 64 - Connectivity Mode Pin Description and Switching Levels

CT Mode Pins		Pin Name During Normal Memory Operation	Switching Level	Notes
Test Enable		TEN	CMOS (20%/80% V_{DD})	1, 2
Chip Select		CS_n	V_{REFCA} ± 200mV	3
Test Input	A	BA[1:0], BG[1:0], A[9:0], A10/AP, A11, A12/BC_n, A13, WE_n/ A14, CAS_n/A15, RAS_n, CKE, ACT_n, ODT, CLK_t, CLK_c, PAR	V_{REFCA} ± 200mV	3,7
	B	LDM_n/LDBI_n, UDM_n/LDBI_n; DM_n/DBI_n	V_{REFDQ} ± 200mV	4
	C	ALERT_n	CMOS (20%/80% V_{DD})	2, 5
	D	RESET_n	CMOS (20%/80% V_{DD})	2
Test Output		DQ[15:0], UDQS_t, UDQS_c, LDQS_t, LDQS_c; DQS_t, DQS_c	V_{TT} ± 100mV	6

Notes:

1. TEN: Connectivity test mode is active when TEN is HIGH and inactive when TEN is LOW. TEN must be LOW during normal operation.
2. CMOS is a rail-to-rail signal with DC HIGH at 80% and DC LOW at 20% of V_{DD} (960mV for DC HIGH and 240mV for DC LOW.)
3. V_{REFCA} should be $V_{DD}/2$.
4. V_{REFDQ} should be $V_{DDQ}/2$.
5. ALERT_n switching level is not a final setting.
6. V_{TT} should be set to $V_{DD}/2$.
7. CK_t and CK_c must be complementary during Connectivity Test maintaining differentail input.

12.12.1 Minimum Terms Definition for Logic Equations

The test input and output pins are related by the following equations, where INV denotes a logical inversion operation and XOR a logical exclusive OR operation:

MT0 = XOR (A1, A6, PAR)
MT1 = XOR (A8, ALERT_n, A9)
MT2 = XOR (A2, A5, A13)
MT3 = XOR (A0, A7, A11)
MT4 = XOR (CK_c, ODT, CAS_n/A15)
MT5 = XOR (CKE, RAS_n, A10/AP)
MT6 = XOR (ACT_n, A4, BA1)
MT7 = x16: XOR (DMU_n/DBIU_n , DML_n/DBIL_n, CK_t)
= x8: XOR (BG1, DML_n/DBIL_n, CK_t)
MT8 = XOR (WE_n/A14, A12/BC, BA0)
MT9 = XOR (BG0, A3, (RESET_n & TEN))
In Connectivity Test Mode, the inputs CK_t and CK_c need to remain complements of each other (CK_c = ~CK_t); this restriction is not part of the JEDEC DDR4 spec

12.12.2 Logic Equations for x8 Operation

DQ0 = MT0 DQ5 = MT5
DQ1 = MT1 DQ6 = MT6
DQ2 = MT2 DQ7 = MT7
DQ3 = MT3 DQS_t = MT8
DQ4 = MT4 DQS_c = MT9

12.12.3 Logic Equations for x16 Operation

DQ0 = MT0 DQ10 = !DQ2
DQ1 = MT1 DQ11 = !DQ3
DQ2 = MT2 DQ12 = !DQ4
DQ3 = MT3 DQ13 = !DQ5
DQ4 = MT4 DQ14 = !DQ6

DQ5 = MT5 DQ15 = !DQ7
DQ6 = MT6 LDQS_t = MT8
DQ7 = MT7 UDQS_t = MT9
DQ8 = !DQ0 LDQS_c = !LDQS_t
DQ9 = !DQ1 UDQS_c = !UDQS_t

12.13 CT Input Timing Requirements

Prior to the assertion of the TEN pin, all voltage supplies must be valid and stable. Upon the assertion of the TEN pin HIGH with RESET_n, CKE and CS_n held HIGH; CLK_t, CLK_c, and CKE signals become test inputs within tCTECT_Valid. The remaining CT inputs become valid tCT_Enable after TEN goes HIGH when CS_n allows input to begin sampling, provided inputs were valid for at least tCT_Valid. While in CT mode, refresh activities in the memory arrays are not allowed; they are initiated either externally (autorefresh) or internally (Self-Refresh).

The TEN pin may be asserted after the device has completed power-on. After the device is initialized and V_{REFDQ} is calibrated, CT mode may no longer be used. The TEN pin may be de-asserted at any time in CT mode. Upon exiting CT mode, the states of the memory device are unknown. A full reset of the memory device is required.

After CT mode has been entered, the output signals will be stable within tCT_Valid after the test inputs have been applied as long as TEN is maintained HIGH and CS_n is maintained LOW.

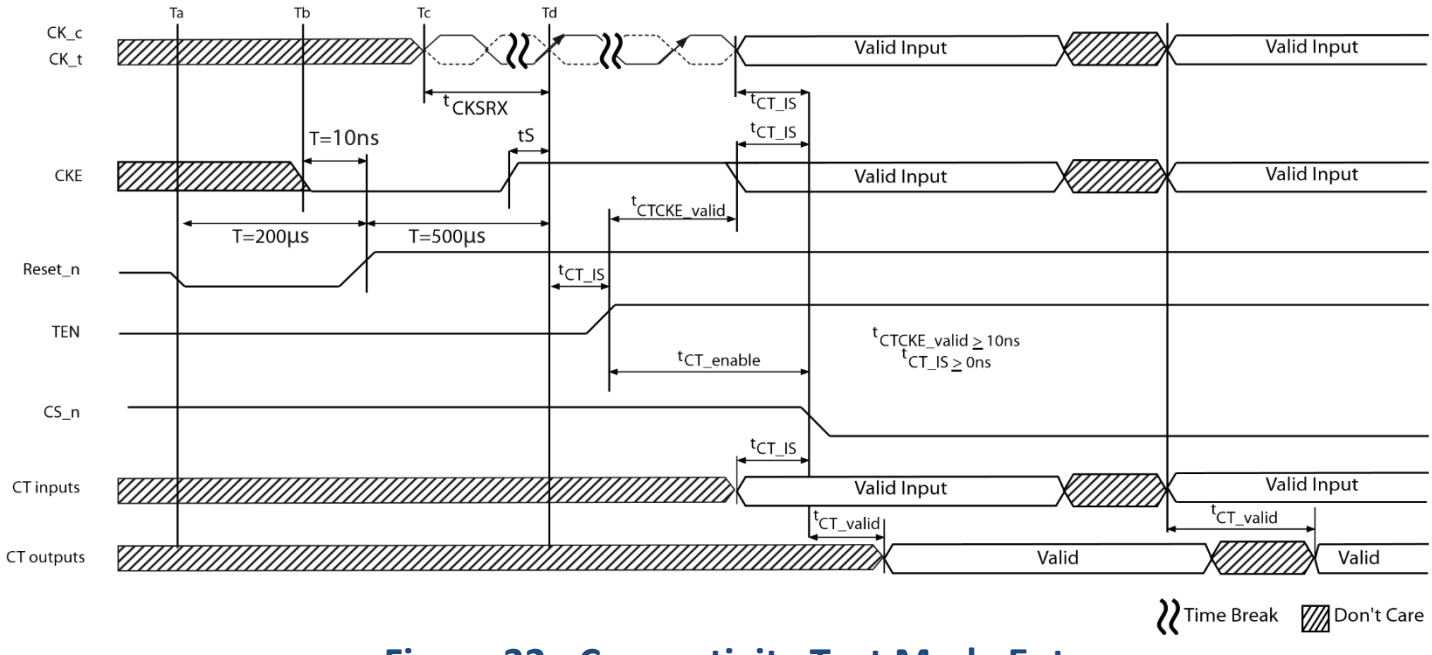

Figure 32 - Connectivity Test Mode Entry

12.14 ACTIVATE Command

The ACTIVATE command is used to open (activate) a row in a particular bank for subsequent access. The values on the BG[1:0] inputs select the bank group, the BA[1:0] inputs select the bank within the bank group, and the address provided on inputs A[15:0] selects the row within the bank. This row remains active (open) for accesses until a PRECHARGE command is issued to that bank.

A PRECHARGE command must be issued before opening a different row in the same bank. Bank-to-bank command timing for ACTIVATE commands use tRRD_S (short) or tRRD_L (long)[1].

Another timing restriction for consecutive ACTIVATE commands [issued at tRRD (MIN)] is tFAW (fourth activate window). Because there is a maximum of four banks in a bank group, the tFAW parameter applies across different bank groups (four ACTIVATE commands issued at tRRD_L (MIN) to the same bank group would be limited by tRC).

Notes:

1. tRRD_S; ACTIVATE-to-ACTIVATE command period (short); applies to consecutive ACTIVATE commands to different bank groups (T0 and T4).
2. tRRD_L; ACTIVATE-to-ACTIVATE command period (long); applies to consecutive ACTIVATE commands in the same bank groups (T4 and T10).

[1] tRRD_S = tRRD_L. See Table 33 – Command and Address Timing for tRRD timing.

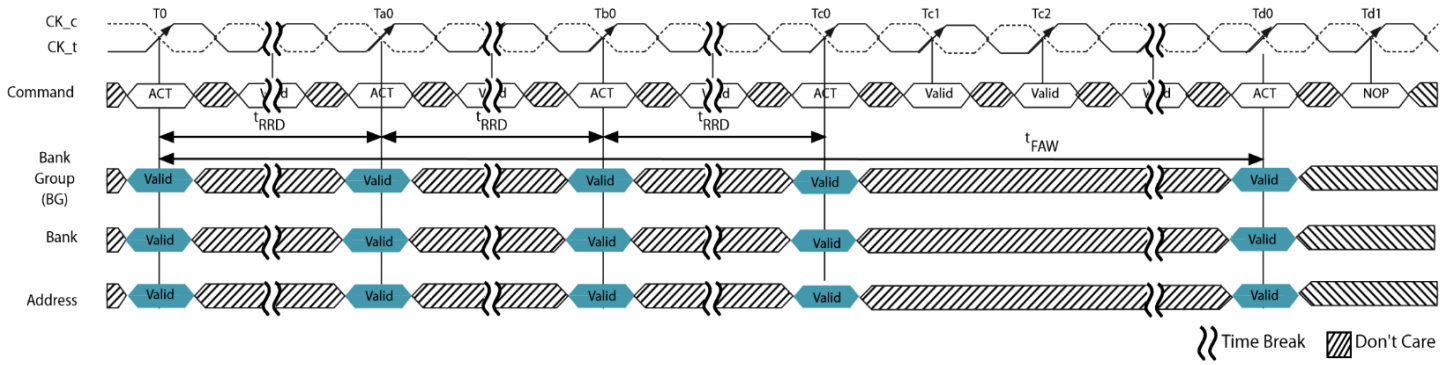

Figure 33 - tFAW Timing

Notes:

1. tFAW; four activate windows.

12.15 PRECHARGE Command

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row activation for a specified time (tRP) after the PRECHARGE command is issued. An exception to this is the case of concurrent auto precharge, where a READ or WRITE command to a different bank is allowed as long as it does not interrupt the data transfer in the current bank and does not violate any other timing parameters.

After a bank is precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. A PRECHARGE command is allowed if there is no open row in that bank (idle state) or if the previously open row is already in the process of precharging. However, the precharge period will be determined by the last PRECHARGE command issued to the bank.

The auto precharge feature is engaged when a READ or WRITE command is issued with A10 HIGH. The auto precharge feature delays the PRECHARGE operation until the READ or WRITE has completed.

12.16 REFRESH Command (store all operation)

REFRESH is required for proper DRAM operation. The store operation is used to finalize the stored write data in in page buffer in all banks. For a x8 device there are 16 banks and 16 page buffers and for a x16 device there are 8 banks and 8 page buffers. When the REFRESH command is issued and MR3[8]=1, the Refresh command executes a store operation of all banks by moving the contents of each page buffer in each bank into the persistent memory array to guarantee persistence. If the REFRESH command is issued and MR3[8] = 0, refresh does not perform a store of all banks operation and is ignored. tRFCmin must meet tST timing. The store operation can use bank staggering (See Table 65 – Bank Staggering Time) to amortize power usage over time.

The bank(s) will not be available for a subsequent row activation for a specified time (tST) after a store operation is in progress.

The Single Bank store operation occurs on is issued with A10 Low and BG and BA determine the bank affected. The store all operation feature is engaged when a store operation is issued with A10 High or a traditional DRAM Refresh command is issued with MR3[A8] = 1. If MR3[A8] = 0, the REFRESH command is ignored.

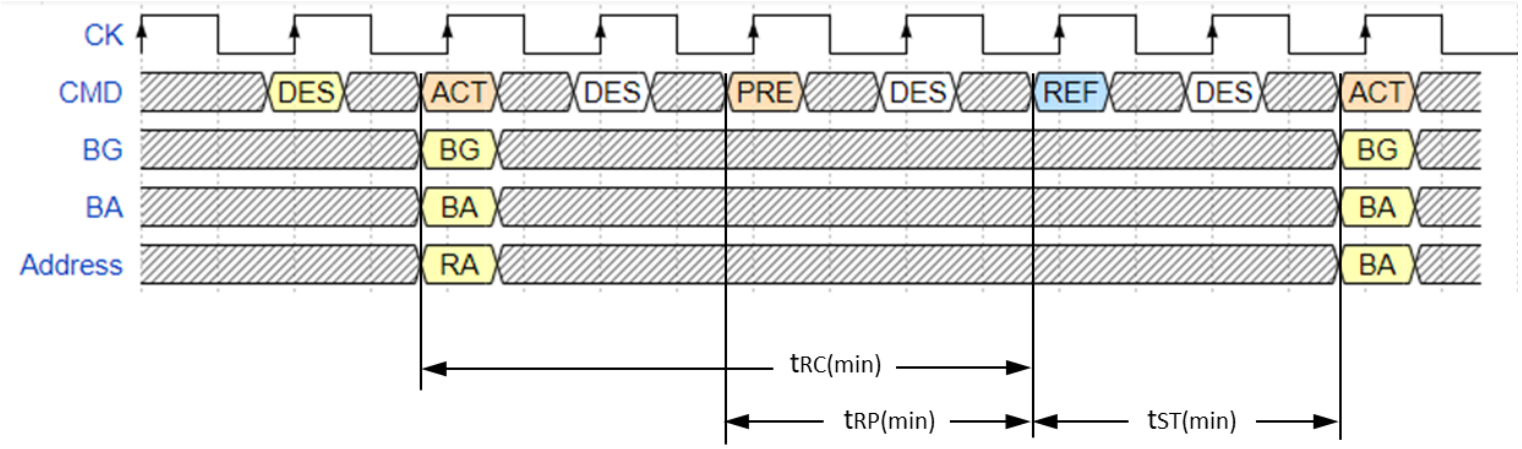

Figure 34 – Refresh Command Timing

12.17 Bank Staggering

To minimize the power required for a store all operation, bank staggering has been implemented to spread the energy requirement out over time. For now, the only supported bank staggering mode is a tST = 380ns or MR3[7:6]=10. When the store all operation is executed, the data in the page buffer of each bank will be moved into the persistent memory array. This action will generate the same power usage as a normal write to the array.

Table 65 – Bank Staggering Time[1]

MR3 [7:6]	Banks/Update (x8)[2]	Banks/Update (x16)[3]	t_{ST} (min)	Unit	Comment
00	2	1	1520	ns	Not supported
01	4	2	760	ns	Not supported
10	8	4	380	ns	Supported
11	16	8	190	ns	Not supported

12.18 SELF-REFRESH Operation

The ST-DDR4 device is non-volatile and does not need to be refreshed. However, the device may use the Self-Refresh command for other functions such as changes in operating frequency and execute the store all operation. While in Self-Refresh mode, a store all operation will automatically be executed until all data has been moved from all pages in all banks into the persistent memory array. If there are no pages to be stored, the Self-Refresh command has no effect. tRFCmin must meet t_{ST} timing. The store all operation can use bank staggering to amortize peak power usage over time.

The Self-Refresh-Entry (SRE) Command is defined by having CS_n, RAS_n, CAS_n/A15, and CKE held low with WE_n/A14 and ACT_n high at the rising edge of the clock.
Before issuing the SRE command, the device must be idle with all banks in the precharge state with tRP satisfied. “Idle state” is defined as: all banks are closed (tRP, tDAL, etc. satisfied), no data bursts are in progress, CKE is high, and all timings from previous operations are satisfied (tMRD, tMOD, tRFC, tZQinit, tZQoper, etc.). Once the SRE command is registered, CKE must be held low to keep the device in Self-Refresh mode. The ST-DDR4 controller automatically disables ODT termination and sets Hi-Z as termination state regardless of the ODT pin and

$R_{TT(PARK)}$ value when it enters into the Self-Refresh mode.
Upon exiting the Self-Refresh mode, the device automatically enables ODT termination and sets $R_{TT(PARK)}$ asynchronously during tXSDLL when $R_{TT(PARK)}$ is enabled.

During normal operation (DLL on) the DLL is automatically disabled upon entering Self-Refresh and is automatically enabled (including a DLL-Reset) upon exiting Self-Refresh.
When the device has entered Self-Refresh mode, all of the external control signals, except CKE and

[1] Bank staggering option is not supported in DLL off mode. During DLL off mode, set MR3[A7:A6]=11.
[2] tST = 16/(Banks/Update) * tRC for x8 devices
[3] tST = 8/(Banks/Update) * tRC for x16 devices

RESET_n, are “don’t care”. For proper Self-Refresh operation, all power supply and reference pins (V_{DD}, V_{DDQ}, V_{SS}, V_{SSQ}, V_{PP}, and V_{REFCA}) must be at valid levels. The device’s internal V_{REFDQ} generator circuitry will remain on. The first WRITE operation or first Write-Leveling activity may not occur earlier than tXS after exit from Self-Refresh.

The clock is internally disabled during Self-Refresh to save power. The minimum time that the device must remain in Self-Refresh mode is tCKESR. The user may change the external clock frequency or halt the external clock tCKSRE after Self-Refresh entry is registered, however, the clock must be restarted and stable tCKSRX before the device can exit Self-Refresh operation.

The procedure for exiting Self-Refresh requires a sequence of events. First, the clock must be stable prior to CKE going back HIGH. Once a Self-Refresh-Exit command (SRX, combination of CKE going high and DESELECT on command bus) is registered, following timing delay must be satisfied:

1. Commands that do not require locked DLL:
   - tXS - ACT, PRE, PREA, REF, SRE, PDE, WR, WRS4, WRS8, WRA, WRAS4, WRAS8,
   - tXS_FAST - ZQCL, MRS commands. For an MRS command, only CL and WR/RTP register and DLL reset in MR0; $R_{TT(NOM)}$ register in MR1; the CWL and $R_{TT(WR)}$ registers in MR2; WRITE and READ preamble registers in MR4; $R_{TT(PARK)}$ register in MR5; tCCD_L/tDLLK and V_{REFDQ} calibration value registers in MR6 are allowed to be accessed provided the device is not in Per Device Addressability (PDA) mode. Access to other ST-DDR4 mode registers must satisfy tXS timing.

2. Commands that require locked DLL:
   - tXSDLL - RD, RDS4, RDS8, RDA, RDAS4, RDAS8, WR, WRS4, WRS8, WRA, WRAS4 and WRAS8

Depending on the system environment and the amount of time spent in Self-Refresh, ZQ Calibration commands may be required to compensate for the voltage and temperature drift as described in “ZQ Calibration Commands” in section 12.25. To issue ZQ Calibration commands, applicable timing requirements must be satisfied.

CKE must remain HIGH for the entire Self-Refresh exit period tXSDLL for proper operation except for Self-
Refresh re-entry. Upon exit from Self-Refresh, the device can be put back into Self-Refresh mode or Power-Down mode after waiting at least tXS. The DESELECT command must be registered on each positive clock edge during the Self-Refresh exit interval tXS. A LOW level must be registered on the ODT pin on each positive clock edge during tXSDLL.

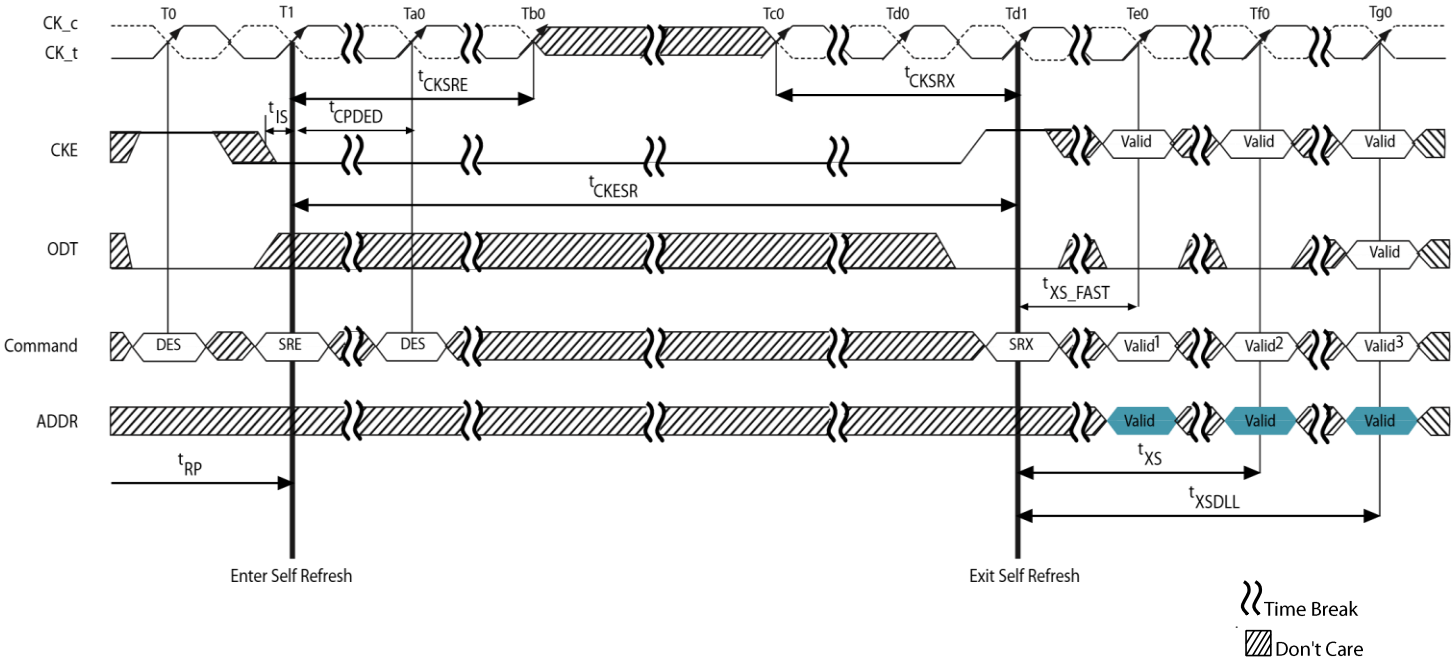

Figure 35 - Self-Refresh Entry/Exit Timing

Notes:

1. Only MRS (limited to those described in the SELF-REFRESH Operation section), or ZQCL commands are allowed.
2. Valid commands not requiring a locked DLL.
3. Valid commands requiring a locked DLL.

12.18.1 Self-Refresh Abort

The Self-Refresh Abort mode is not supported. Upon exit from Self-Refresh, the device requires a minimum of one extra REFRESH (and subsequent store all operation) command before it is put back into Self-Refresh Mode. The exit timing from Self-Refresh exit to first valid command not requiring a locked DLL is tXS. The value of tXS is (tRFC+10ns). This delay is to allow for any refreshes started by the ST-DDR4 device to complete.

12.19 Power-Down Mode

Power-Down is synchronously entered when CKE is registered LOW (along with a Deselect command). CKE is not allowed to go LOW when the following operations are in progress: MRS command, MPR operations, ZQCAL operations, DLL locking, or READ/WRITE operations. CKE is allowed to go LOW while any other operations, such as Row Activation, Precharge or Auto

Precharge, or Refresh, are in progress, but the Power-Down I_{DD} specification will not be applied until those operations are complete.

For the fastest Power-Down exit timing, the DLL should be in a locked state when Power-Down is entered. If the DLL is not locked during Power-Down entry, the DLL must be reset after exiting Power-Down mode for proper READ operation and synchronous ODT. The ST-DDR4 design provides all AC and DC timing and voltage specification as well as proper DLL operation with any CKE intensive operations as long as the controller complies with ST-DDR4 specifications. During Power-Down, if all banks are closed after any in-progress commands are completed, the device will be in Precharge Power-Down mode; if any bank is open after in-progress commands are completed, the device will be in Active Power-Down mode.

Entering Power-Down deactivates the input and output buffers, excluding CK, CKE, and RESET_n.

Note that the device continues to provide $R_{TT(PARK)}$ termination if it is enabled in the mode register MR5[A8:A6]. To protect internal delay on the CKE line to block the input signals, multiple DESELECT commands are needed during the CKE switch off and on cycle(s); this timing period is defined as tCPDED. CKE LOW will result in deactivation of command and address receivers after tCPDED has expired.

Table 66 – Power-Down Entry Definitions

ST-DDR4 Status	DLL	Power-Down Exit	Relevant Parameters
Active (a bank or more open)	On	Fast	tXP to any valid command.
Precharged (all banks precharged)	On	Fast	tXP to any valid command

The DLL is kept enabled during Precharge Power-Down or Active Power-Down. In Power-Down mode, CKE is LOW, RESET_n is HIGH, and a stable clock signal must be maintained at the inputs of the device. If RESET_n goes LOW during Power-Down, the device will be out of Power-Down

mode and in the reset state. CKE LOW must be maintained until tCKE has been satisfied. Power-Down duration is limited by 9 × tREFI.

The Power-Down state is synchronously exited when CKE is registered HIGH (along with DESELECT command). CKE HIGH must be maintained until tCKE has been satisfied. A valid, executable command can be applied with Power-Down exit latency, tXP, and/or tXPDLL, after CKE goes HIGH. Power-Down exit latency is defined in the AC Specifications table.

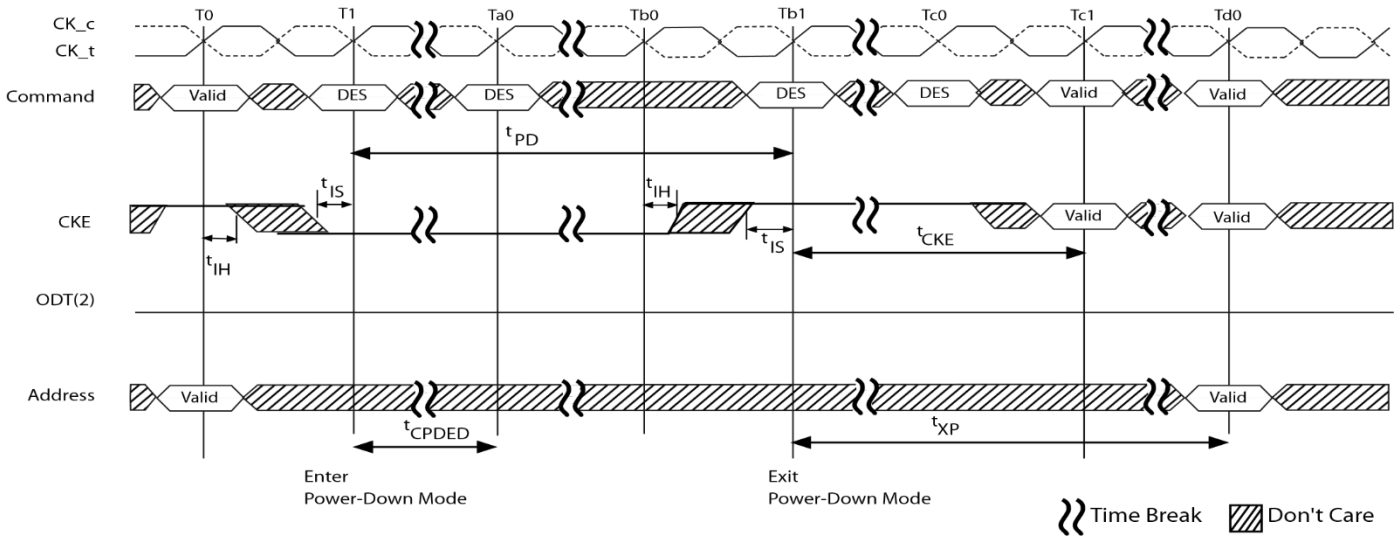

Figure 36 - Active Power Down Entry and Exit Timing MR5 bit = 0

Notes:

1. VALID command at T0 is ACT, DES or Precharge with still one bank remaining open after completion of the precharge command.
2. ODT pin driven to a valid state. MR5 bit A5=0 (default setting) is shown.

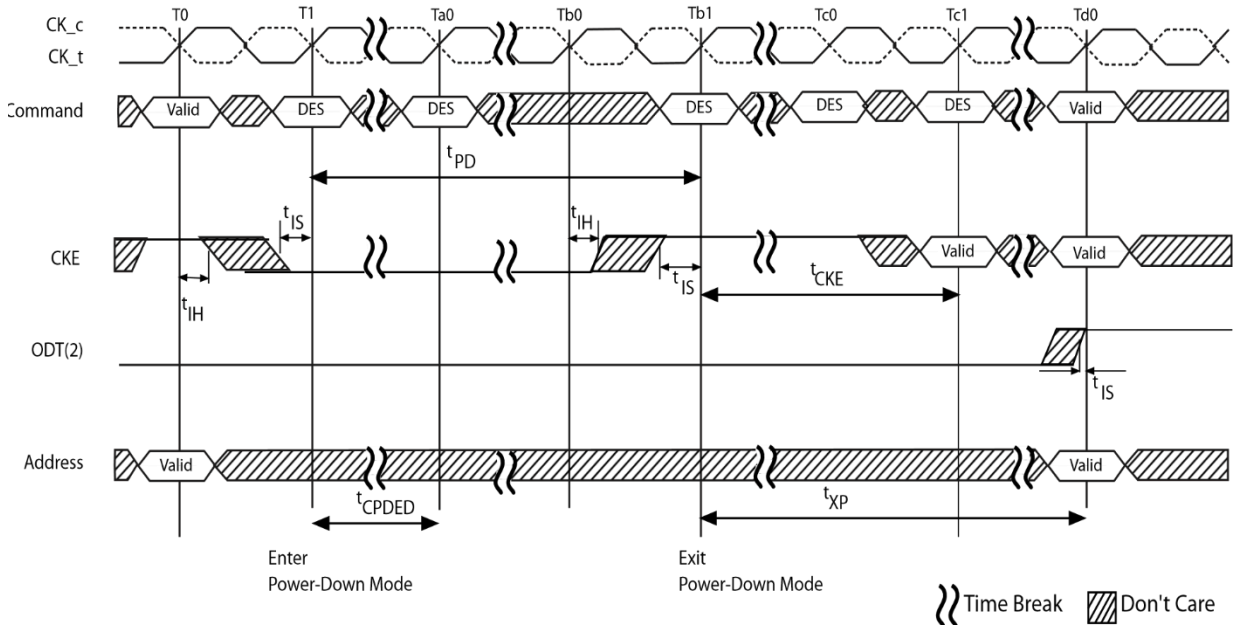

Figure 37 - Active Power Down Entry and Exit Timing MR5 bit = 1

Notes:

1. VALID command at T0 is ACT, DES or Precharge with still one bank remaining open after completion of the precharge command.

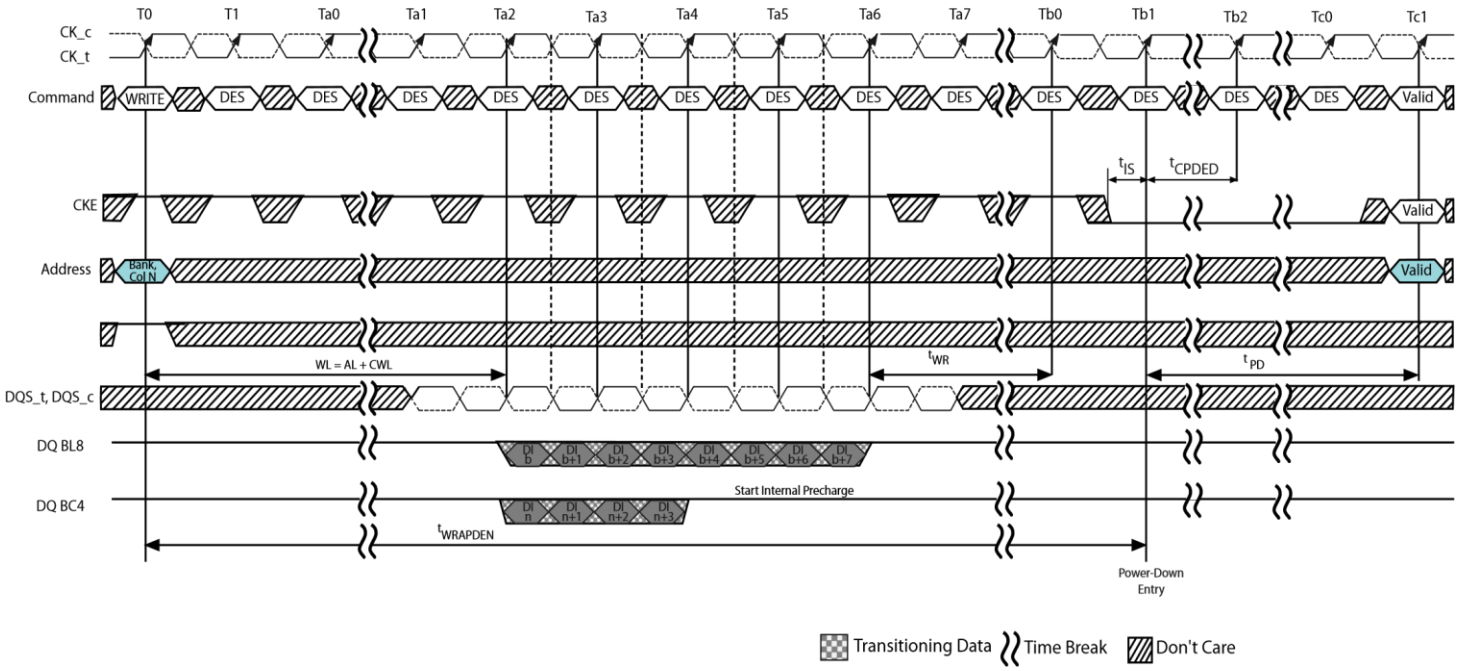

Figure 38 - Power-Down Entry After Write and Write with Auto Precharge

Notes:

1. DI n (or b) = data-in from column n (or b).
2. Valid commands at T0 are ACT, DES, or PRE with one bank remaining open after completion of the PRECHARGE command.

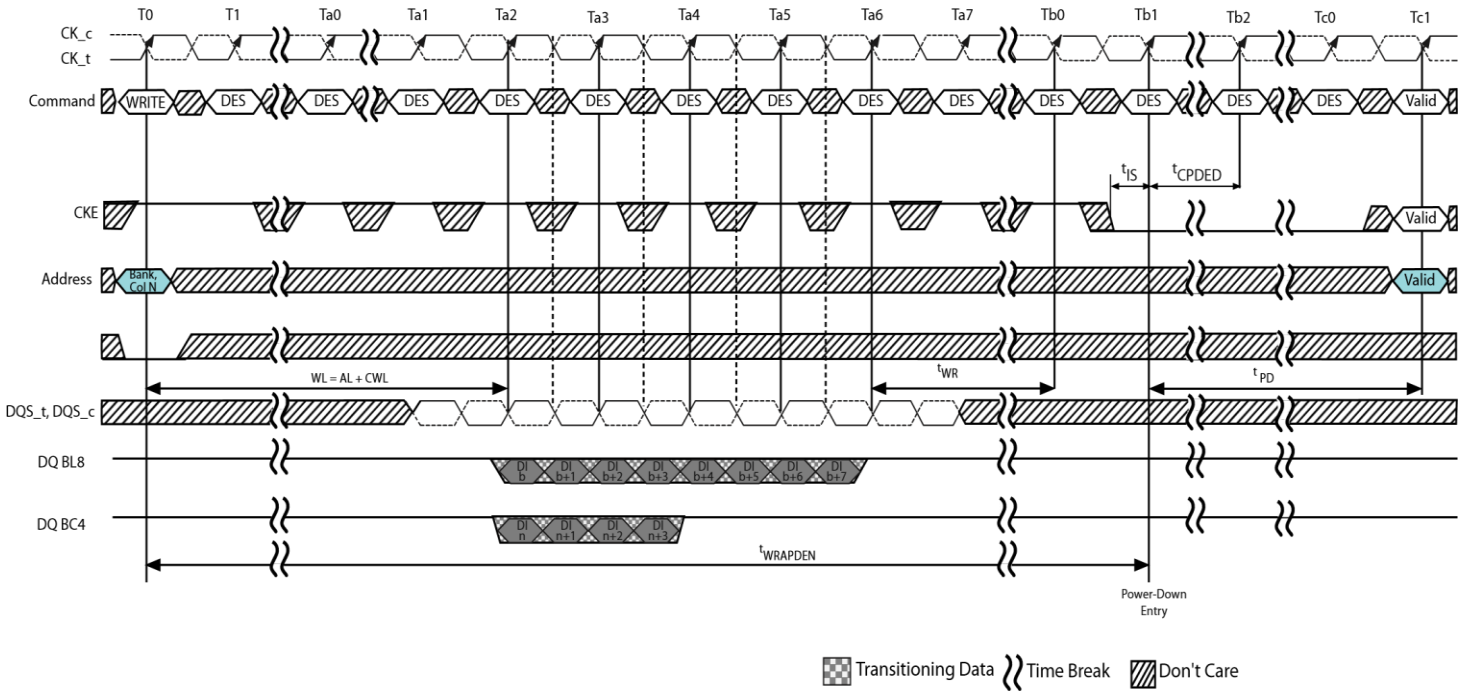

Figure 39 - Power-Down Entry After Write

Notes:

1. DI n (or b) = data-in from column n (or b).

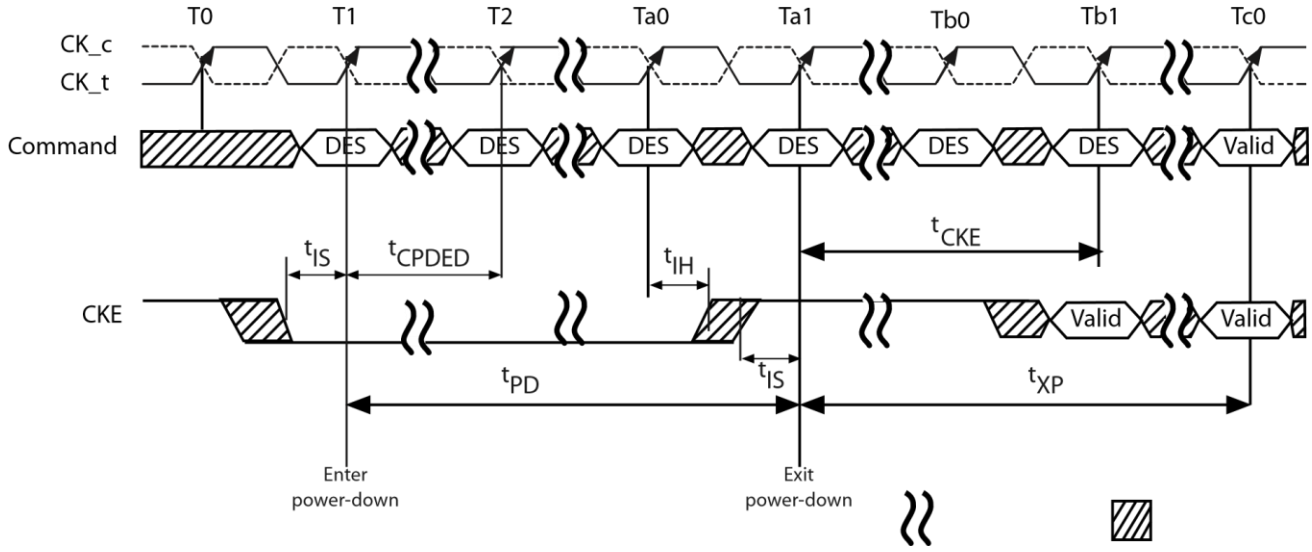

Figure 40 - Precharge Power-Down Entry and Exit

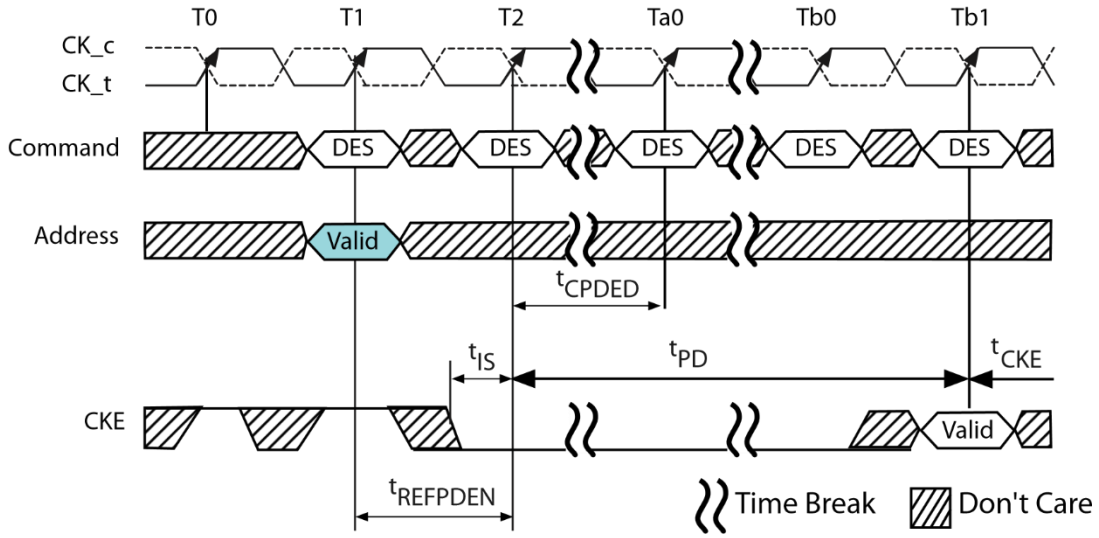

Figure 41 - REFRESH Command to Power-Down Entry

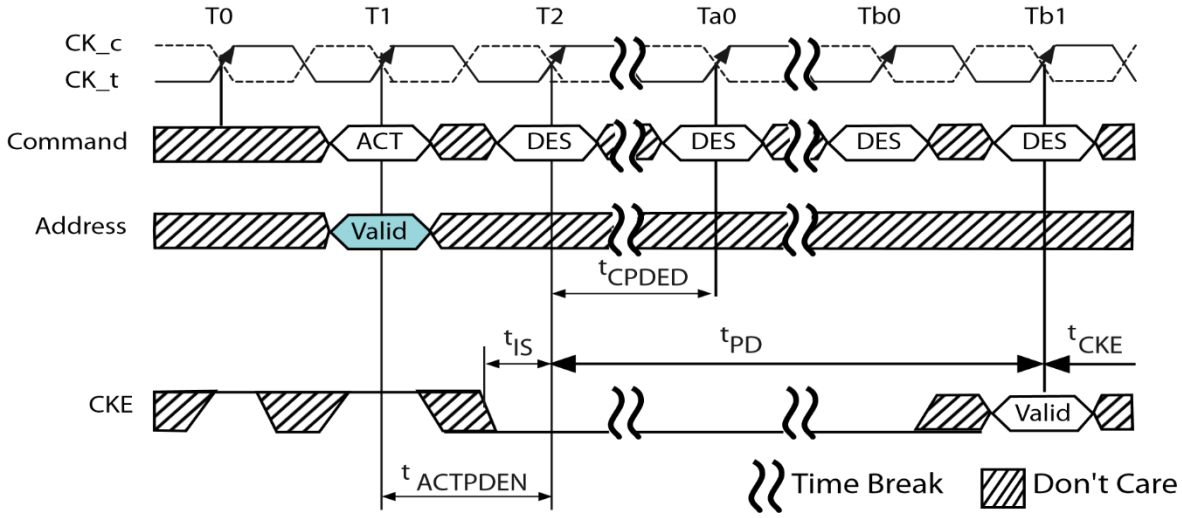

Figure 42 - ACTIVE Command to Power-Down Entry

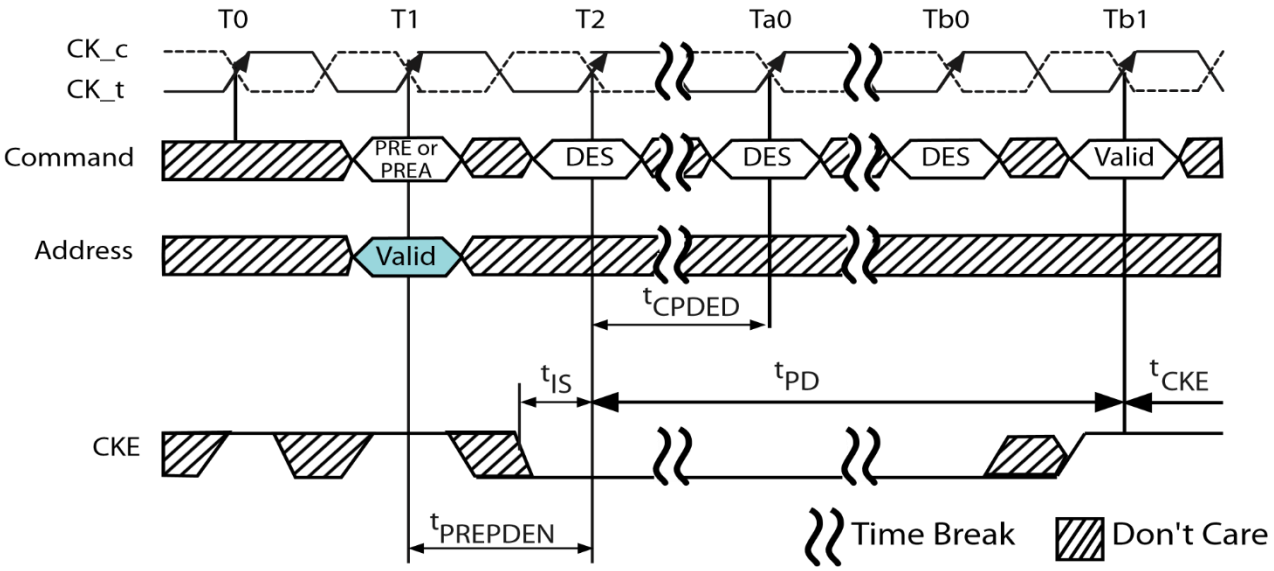

Figure 43 - PRECHARGE/PRECHARGE ALL Command to Power-Down Entry

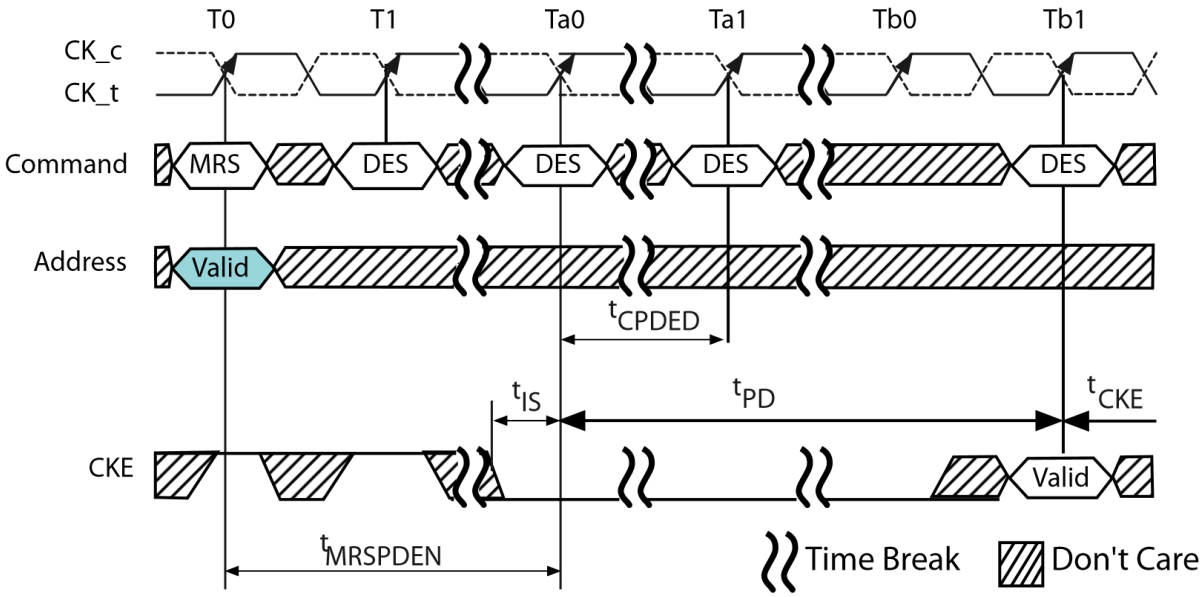

Figure 44 - MRS Command to Power-Down Entry

12.20 Data Mask

The DATA MASK (DM) function, also described as PARTIAL WRITE, is supported for x8 and x16 configurations. The DM function shares a common pin with the DBI_n and TDQS functions. The DM function applies only to WRITE operations and cannot be enabled at the same time the WRITE DBI function is enabled. The valid configurations for the TDQS, DM, and DBI functions are shown here.

Table 67 - Data Masking

Data Mask (DM) MR5[A10]	TDQS (x8 only) MR1[A11]	Write DBI 1 MR5[A11]
Enabled	Disabled	Disabled
Disabled	Enabled	Disabled
	Disabled	Disabled

Note:

1. Data Bus Inversion is not supported, however the Mode Registers should be set according to this table with Write DBI always disabled.

When enabled, the DM function applies during a WRITE operation. If DM_n is sampled LOW on a given byte lane, the device masks the write data received on the DQ inputs. If DM_n is sampled HIGH on a given byte lane, the device does not mask the data and writes this data into the device core. The DQ frame format for x8 and x16 configurations is shown below.

Table 68 - Data Mask, DQ Frame Format (x8)

Function	Transfer							
	0	1	2	3	4	5	6	7
DQ[7:0]	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
DM_n	DM0	DM1	DM2	DM3	DM4	DM5	DM6	DM7

Table 69 - Data Mask, DQ Frame Format (x16)

Function	Transfer							
	0	1	2	3	4	5	6	7
DQ[7:0]	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
LDM_n	LDM0	LDM1	LDM2	LDM3	LDM4	LDM5	LDM6	LDM7
DQ[15:8]	UByte 0	UByte 1	UByte 2	UByte 3	UByte 4	UByte 5	UByte 6	UByte 7
UDM_n	UDM0	UDM1	UDM2	UDM3	UDM4	UDM5	UDM6	UDM7

12.21 Programmable Preamble Modes and DQS Postamble

The ST-DDR4 device does not support programmable WRITE and READ preamble modes. Only the normal 1tCK preamble mode is supported. The 2tCK preamble mode places special timing constraints on many operational features as well as being supported for data rates of DDR4-2666 and faster.

READ preamble training is supported; this mode can be used by the ST-DDR4 controller to train or “read level” the DQS receivers.

12.21.1 WRITE Preamble Mode

Only 1tCK mode is supported.

12.21.2 READ Preamble Mode

Only 1tCK mode is supported.

12.21.3 READ Preamble Training

DDR4 supports READ preamble training via MPR reads; that is, READ preamble training is allowed only when the device is in the MPR access mode. The READ preamble training mode can be used by the ST-DDR4 controller to train or “read level” its DQS receivers. READ preamble training is entered via an MRS command (MR4[10] = 1 is enabled and MR4[10] = 0 is disabled). After the MRS command is issued to enable READ preamble training, the device’s DQS signals are driven to a valid level by the time tSDO is satisfied. During this time, the data bus DQ signals are held quiet, which is, driven HIGH. The DQS_t signal remains driven LOW and the DQS_c signal remains driven HIGH until an MPR Page0 READ command is issued (MPR0 through MPR3 determine which pattern is used), and when CAS latency (CL) has expired, the DQS signals will toggle normally depending on the burst length setting. To exit READ preamble training mode, an MRS command must be issued, MR4[10] = 0.

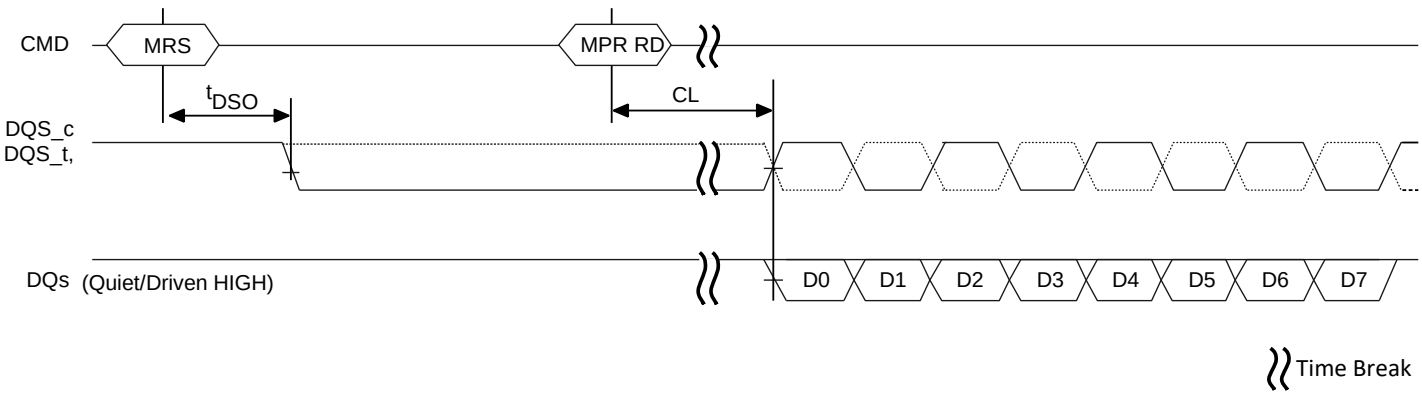

Figure 45 - READ Preamble Training

12.21.4 WRITE Postamble

WRITE Postamble is 0.5tCK.

12.21.5 READ Postamble

WRITE Postamble is 0.5tCK.

12.22 READ Operation

12.22.1 READ Timing Definitions

The read timings shown below are applicable in normal operation mode, that is, when the DLL is enabled and locked.

Note: tDQSQ = both rising/falling edges of DQS; no tAC defined.
Rising data strobe edge parameters:

- tDQSCK (MIN)/(MAX) describes the allowed range for a rising data strobe edge relative to CK.
- tDQSCK is the actual position of a rising strobe edge relative to CK.
- tQSH describes the DQS differential output HIGH time.
- tDQSQ describes the latest valid transition of the associated DQ pins.
- tQH describes the earliest invalid transition of the associated DQ pins.
- Falling data strobe edge parameters:
- tQSL describes the DQS differential output LOW time.
- tDQSQ describes the latest valid transition of the associated DQ pins.
- tQH describes the earliest invalid transition of the associated DQ pins.

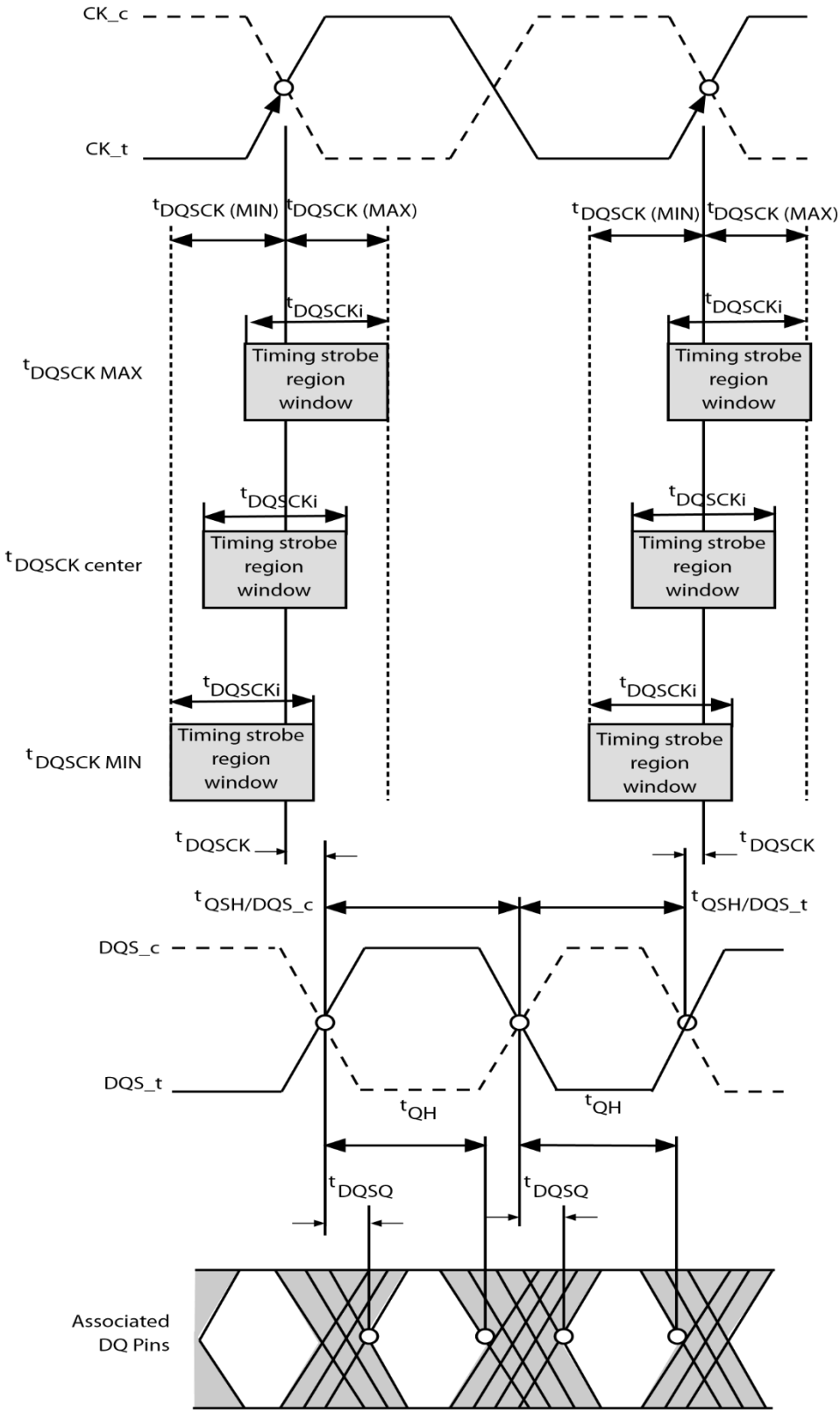

Figure 46 - READ Timing Definitions

12.22.2 READ Timing – Clock-to-Data Strobe Relationship

The clock-to-data strobe relationship shown below is applicable in normal operation mode, that is when the DLL is enabled and locked.

Rising Data Strobe Parameters:

- $t_{DQSCK\ (MIN)/(MAX)}$ describes the allowed range for a rising data strobe edge relative to CK.
- t_{DQSCK} is the actual position of a rising strobe edge relative to CK.
- tQSH describes the data strobe high pulse width.
- tHZ(DQS) DQS strobe going to high, non-drive level (Shown in the Postamble section of the Figure below.)

Falling data strobe edge parameters:

- tQSL describes the data strobe low pulse width.
- tLZ(DQS) DQS strobe going to low, initial drive level (Shown in the Preamble section of the Figure below.)

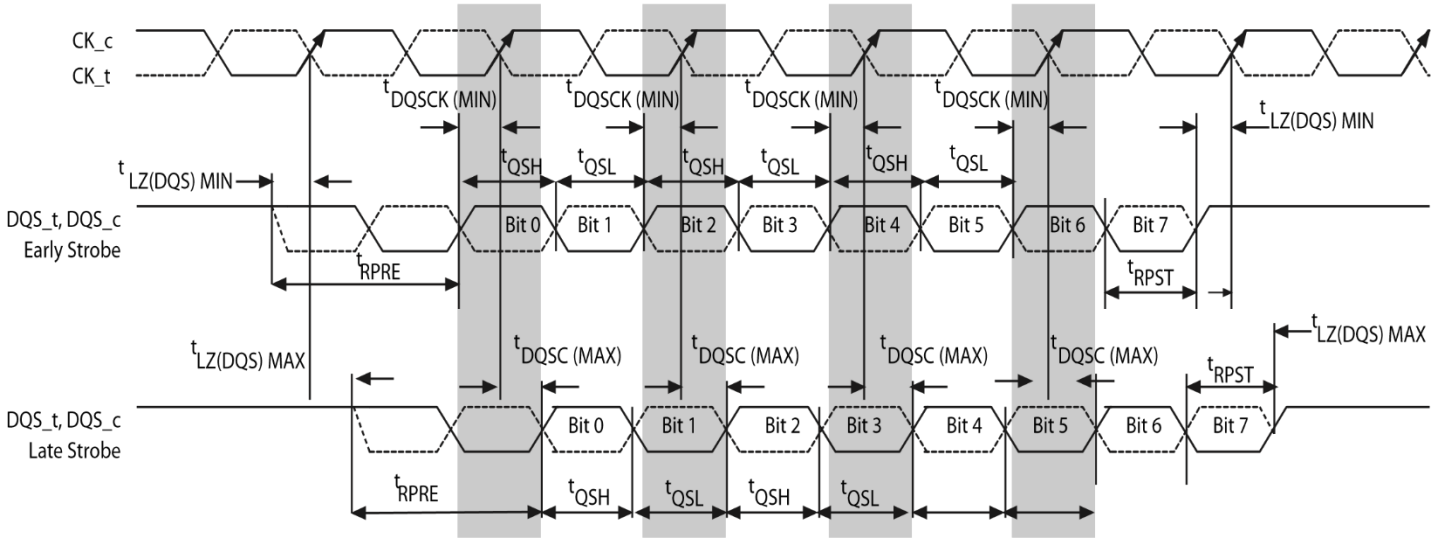

Figure 47 – Clock-to-Data Strobe Relationship

Notes:

1. Within a burst, the rising strobe edge will vary within tDQSCKj while at the same voltage and temperature. However, when the device, voltage, and temperature variations are incorporated, the rising strobe edge variance window can shift between tDQSCK (MIN) and tDQSCK (MAX).
2. A timing of this window's right edge (latest) from rising CK_t, CK_c is limited by a device's actual tDQSCK (MAX). A timing of this window's left inside edge (earliest) from rising CK_t, CK_c is limited by tDQSCK (MIN).
3. Notwithstanding note 1, a rising strobe edge with tDQSCK (MAX) at T(n) cannot be immediately followed by a rising strobe edge with tDQSCK (MIN) at T(n + 1) because other timing relationship (tQSH, tQSL) exist: if tDQSCK(n + 1) <0: tDQSCK(n) < 1.0 tCK - (tQSH (MIN) + tQSL (MIN)) - | tDQSCK(n + 1) |.

4. The DQS_t, DQS_c differential output HIGH time is defined by tQSH, and the DQS_t, DQS_c differential output LOW time is defined by tQSL.
5. tLZ(DQS) MIN and tHZ(DQS) MIN are not tied to tDQSCK (MIN) (early strobe case), and tLZ (DQS) MAX and tHZ(DQS) MAX are not tied to tDQSCK (MAX) (late strobe case).
6. The minimum pulse width of READ preamble is defined by tRPRE (MIN).
7. The maximum READ postamble is bound by tDQSCK (MIN) plus tQSH (MIN) on the left side and tHZDSQ (MAX) on the right side.
8. The minimum pulse width of READ postamble is defined by tRPST (MIN).
9. The maximum READ preamble is bound by tLZDQS (MIN) on the left side and tDQSCK (MAX) on the right side.

12.22.3 READ Timing - Data Strobe-to-Data Relationship

The data strobe-to-data relationship is shown below and is applied when the DLL is enabled and locked.

Note: tDQSQ: both rising/falling edges of DQS; no tAC defined.

Rising data strobe edge parameters:

- tDQSQ describes the latest valid transition of the associated DQ pins.
- tQH describes the earliest invalid transition of the associated DQ pins. Falling data strobe edge parameters:
- tDQSQ describes the latest valid transition of the associated DQ pins.
- tQH describes the earliest invalid transition of the associated DQ pins. Data valid window parameters:
- tDVWd is the data valid window per device and is derived from the smallest (earliest) observable tQH minus the largest (slowest) observable tDQSQ on a given device.
- tDVWp is the data valid window per pin per device and is derived by determining the tDVWd component for each of the device's data output.

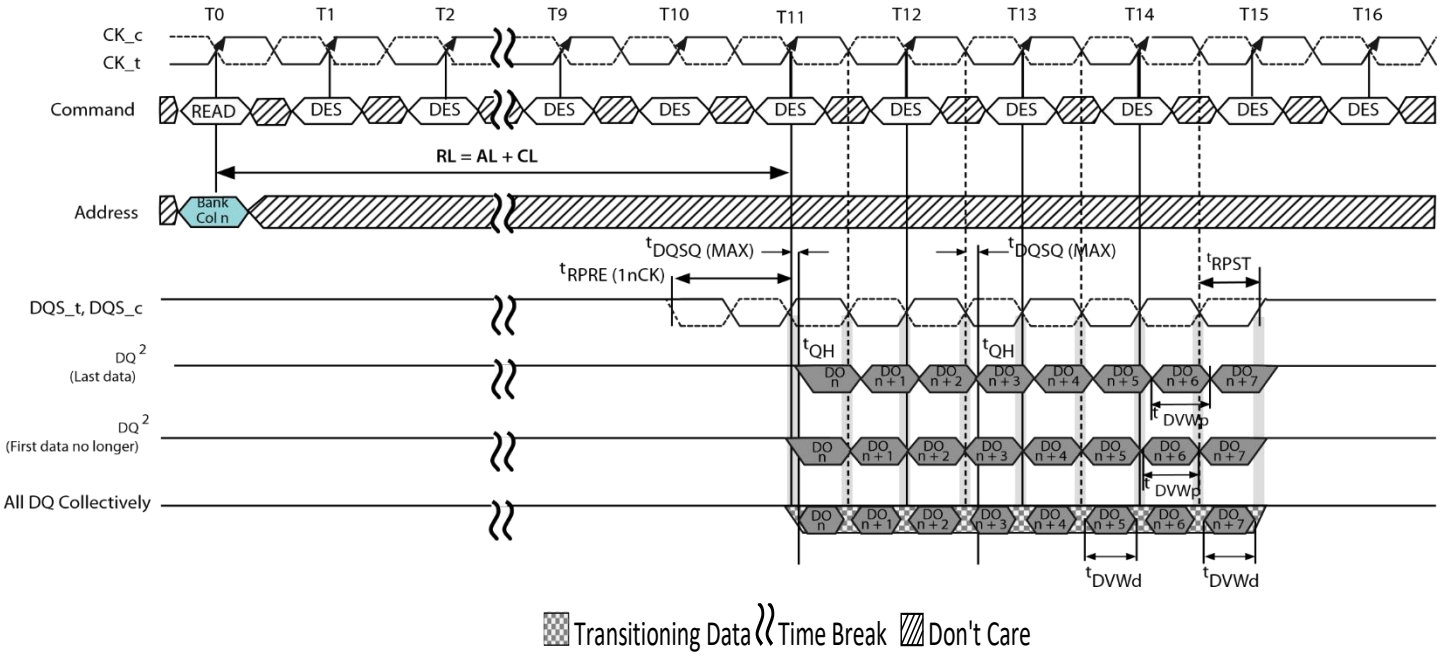

Figure 48 - Data Strobe-to-Data Relationship

Notes:

1. BL = 8, RL = 10 (AL = 0, CL = 1), Preamble = 1tCK.
2. D_{OUT}n = data-out from column n.
3. DES commands are shown for ease of illustration; other commands may be valid at these times
4. BL8 setting activated by either MR0[a1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during READ commands at T0.
5. Output timings are referenced to V_{DDQ}, and DLL on for locking.
6. tDQSQ defines the skew between DQS to data and does not define DQS to clock.
7. Early data transitions may not always happen at the same DQ. Data transitions of a DQ can vary (either early or late) within a burst.

12.22.4 LZ(DQS), tLZ(DQ), tHZ(DQS), and tHZ(DQ) Calculations

tHZ and tLZ transitions occur in the same time window as valid data transitions. These parameters are referenced to a specific voltage level that specifies when the device output is no longer driving tHZ(DQS) and tHZ(DQ), or begins driving tLZ(DQS) and tLZ(DQ). The figure below shows a method to calculate the point when the device is no longer driving tHZ(DQS) and tHZ(DQ), or begins driving tLZ(DQS) and tLZ(DQ), by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent. tLZ(DQS), tLZ(DQ), tHZ(DQS), and tHZ(DQ) are defined as singled-ended parameters.

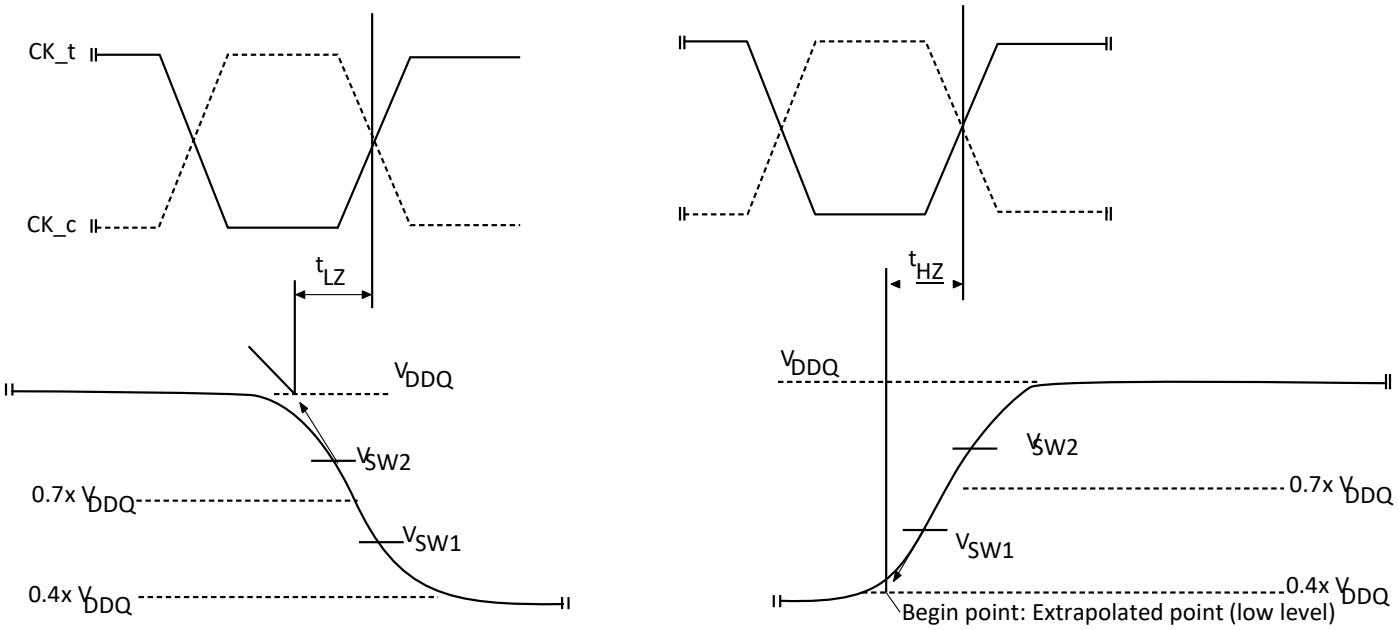

Figure 49 - tLZ, and tHZ(DQS) Method for Calculating Transitions and Endpoints

Notes:

1. V_{SW1} = (0.70 - 0.04) x V_{DDQ} for both tLZ and tHZ
2. V_{SW2} = (0.70 - 0.04) x V_{DDQ} for both tLZ and tHZ
3. Extrapolated point (low level) = V_{DDQ}/(50 + 34) x 34 = 0.4 x V_{DDQ}
4. Driver Impedence = RZQ/7 = 34 Ω
5. V_{TT} test load = 50 Ω to V_{DDQ}
6. tLZ(DQ): CK_t, CK_c rising crossing at RL (left diagram)
7. tHZ(DQ) with BL8; CK_t, CK_c rising crossing at RL + 4CK (right diagram)
8. tHZ(DQ) with BC4; CK_t, CK_c rising crossing at RL + 2CK (right diagram)

12.22.4.1 RPRE Calculation

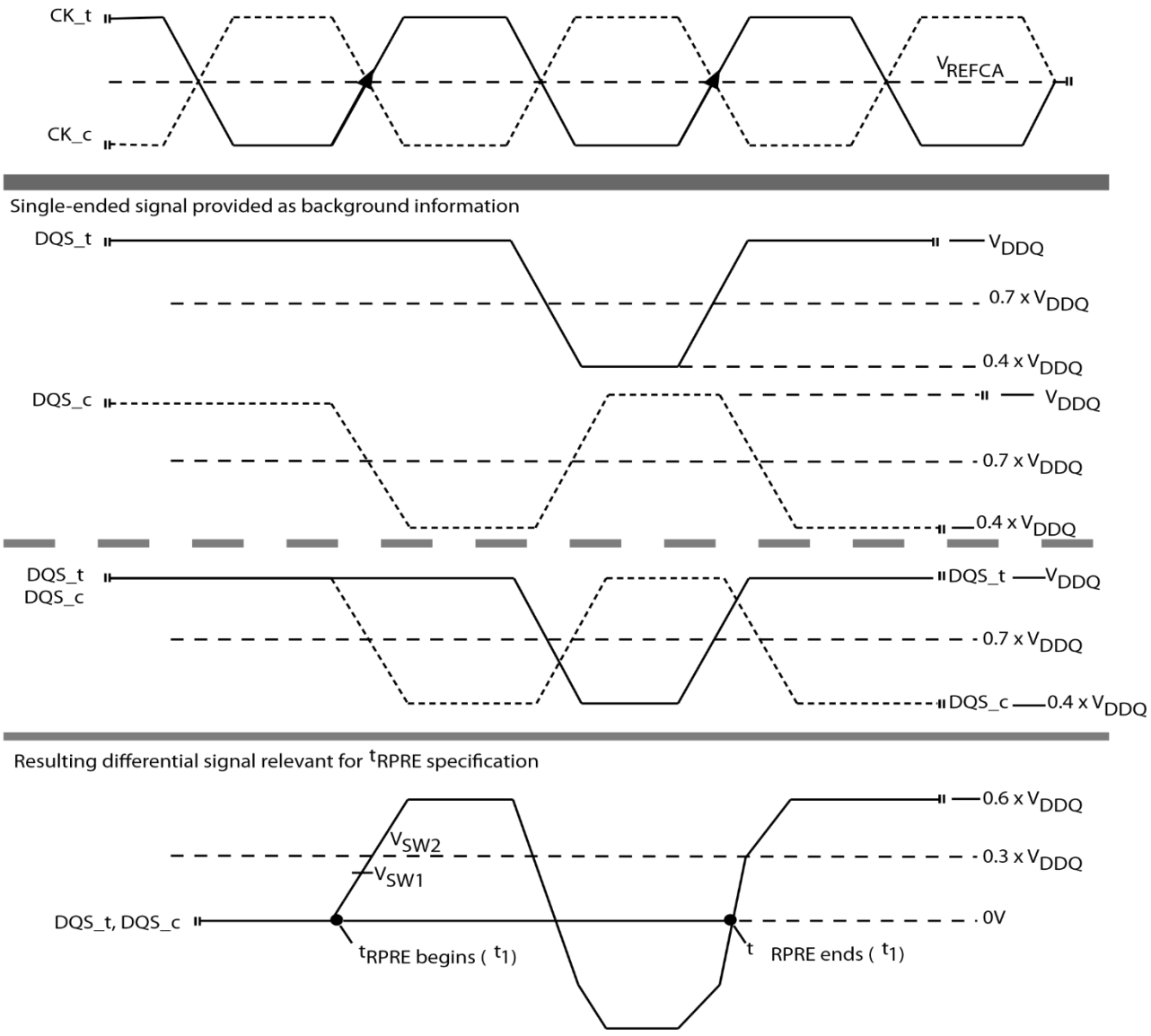

Figure 50 - tRPRE Method for Calculating Transisitions and Endpoints

Notes:

1. V_{SW1} = (0.03 - 0.04) x V_{DDQ}
2. V_{SW2} = (0.30 + 0.04) x V_{DDQ}
3. DQS_t and DQS_c low level = V_{DDQ}/(50 + 34) x 34 = 0.4 x V_{DDQ}
4. Driver Impedance = RZQ/7 = 34 Ω
5. V_{TT} test load = 50 Ω to V_{DDQ}

12.22.4.2 RPST Calculation

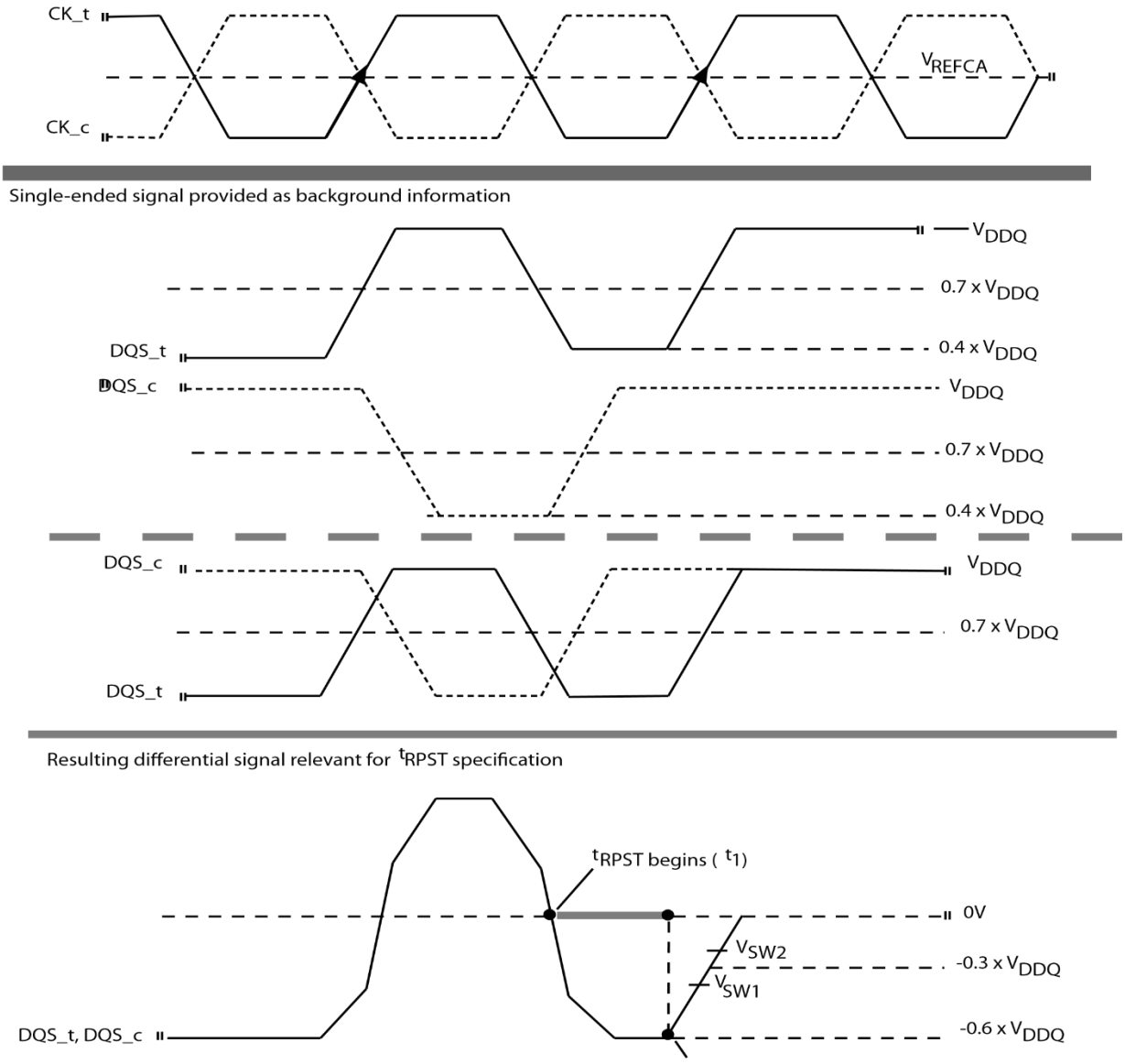

Figure 51 - tRPST Method for Calculating Transisitions and Endpoints

Notes:

1. t RPST ends (2)t
2. V_{SW1} = (-0.03 - 0.04) x V_{DDQ}
3. V_{SW2} = (-0.30 + 0.04) x V_{DDQ}
4. DQS_t and DQS_c low level = V_{DDQ}/(50 + 34) x 34 = 0.4 x V_{DDQ}
5. Driver Impedance = RZQ/7 = 34 Ω
6. V_{TT} test load = 50 Ω to V_{DDQ}

12.22.5 READ Burst Operation

DDR4 READ commands support bursts of BL8 (fixed), BC4 (fixed), and BL8/BC4 on-the-fly (OTF); OTF uses address A12 to control OTF when OTF is enabled:

- A12 = 0, BC4 (BC4 = burst chop)
- A12 = 1, BL8

READ commands can issue precharge automatically with a READ with auto precharge command (RDA), and is enabled by A10 HIGH:

- READ command with A10 = 0 (RD) performs standard read, bank remains active after READ burst.
- READ command with A10 = 1 (RDA) performs read with auto precharge, bank goes into precharge after READ burst.

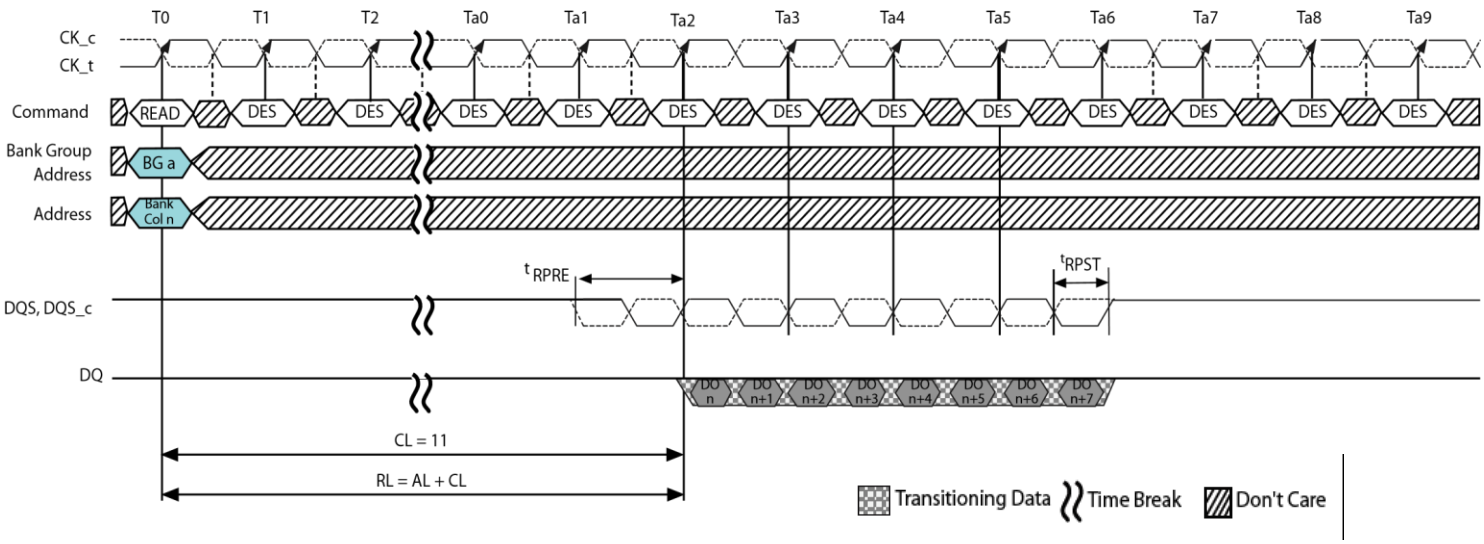

Figure 52 - READ Burst Operation, RL = 10 (CL = 10, BL8)

Notes:

1. BL8, RL = 0, AL = 0, CL = 10, Preamble = 1tCK
2. DO *n* = data-out from column *n*
3. DES commands are shown for ease of illustration; other commands may be valid at these times
4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during READ command at T0.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable.

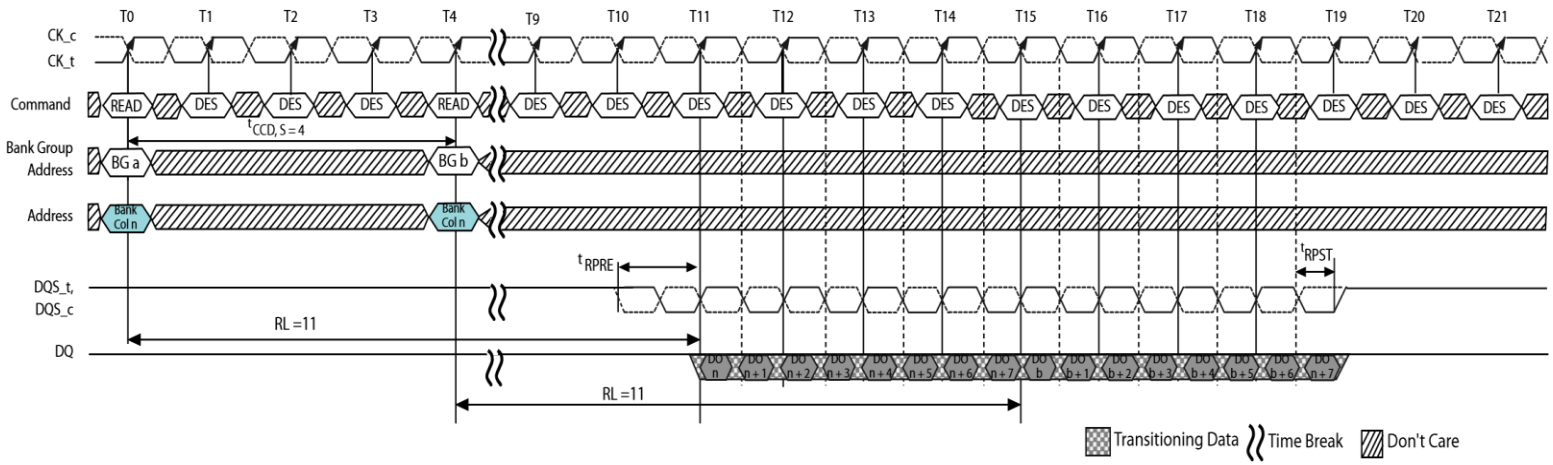

Figure 53 - Consecutive READ (BL8) with 1tCK Preamble in Different Bank Group

Notes:

1. BL8, AL = 0, CL = 10, Preamble = 1tCK
2. DO *n* (or *b*) = data-out from column *n* (or column *b*)
3. DES commands are shown for ease of illustration; other commands may be valid at these times
4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during READ commands at T0 and T4.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable.

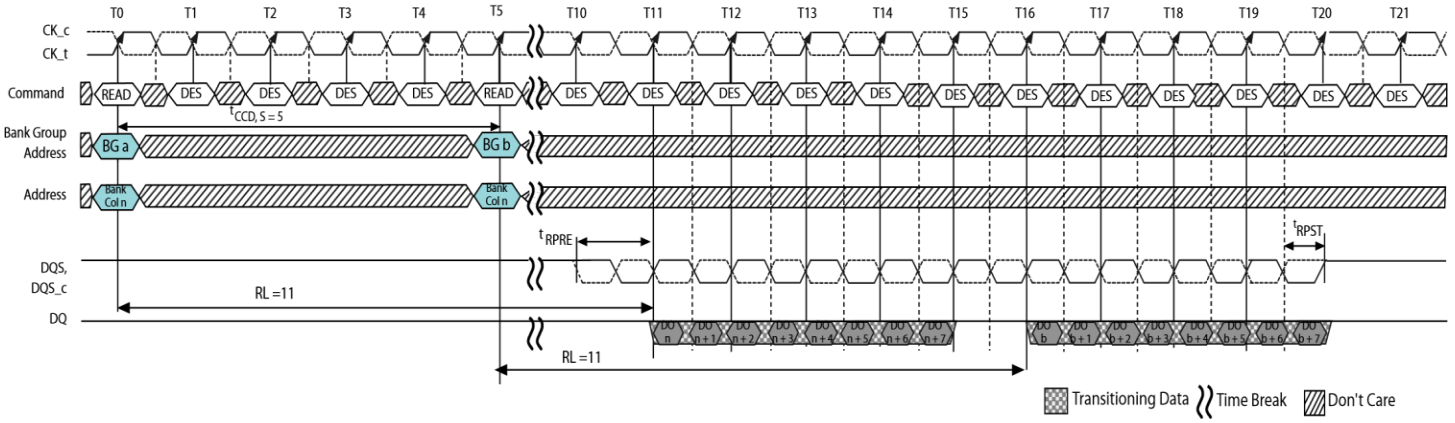

Figure 54 - Non-Consecutive READ (BL8) with 1tCK Preamble in Same or Different Bank Group

Notes:

1. BL8, AL = 0, CL = 10, Preamble = 1tCK, tCCD_S/L = 5.
2. DO *n* (or *b*) = data-out from column *n* (or column *b*)
3. DES commands are shown for ease of illustration; other commands may be valid at these times
4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during READ commands at T0 and T5.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable.

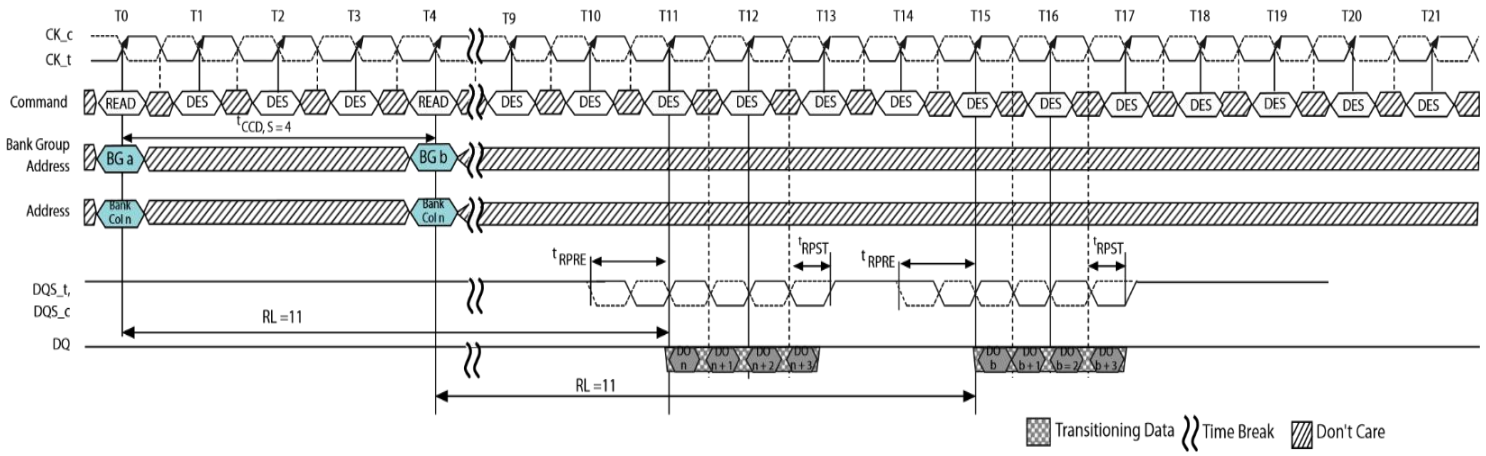

Figure 55 - READ (BC4) to READ (BC4 with 1tCK Preamble in Different Bank Group

Notes:

1. BL8, AL = 0, CL = 10, Preamble = 1tCK.
2. DO *n* (or *b*) = data-out from column *n* (or column *b*)
3. DES commands are shown for ease of illustration; other commands may be valid at these times
4. BC4 setting activated by either MR0[1:0] = 10 or MR0[1:0] = 01 and A12 = 0 during READ commands at T0 and T4.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable.

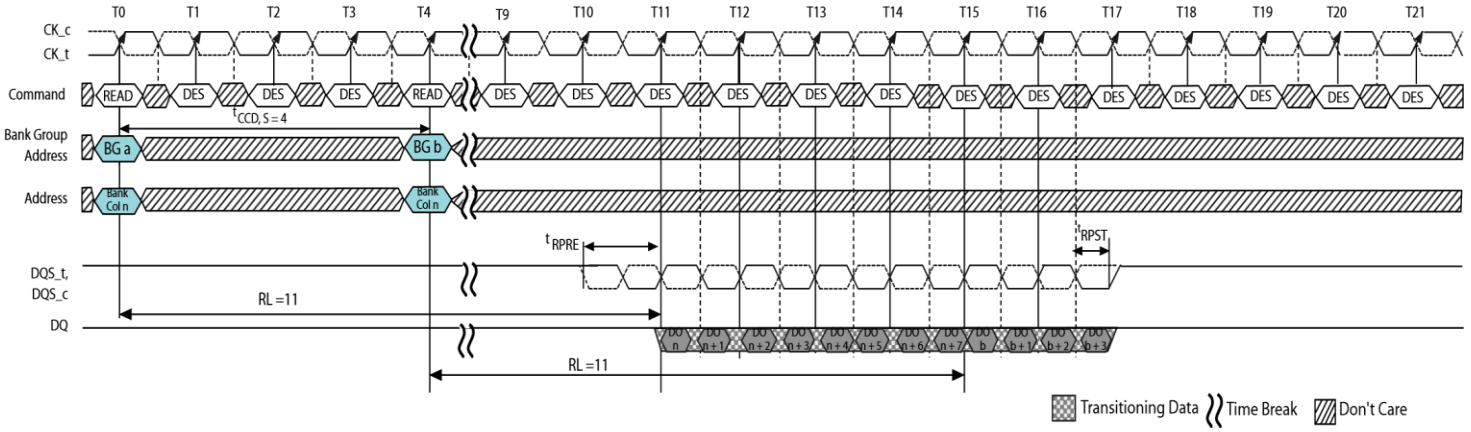

Figure 56 - READ (BL8) to READ (BC4) OTF with 1tCK Preamble in Different Bank Group

Notes:

1. BL = 8, AL = 0, CL = 10, Preamble = 1tCK.
2. DO *n* (or *b*) = data-out from column *n* (or column *b*)
3. DES commands are shown for ease of illustration; other commands may be valid at these times
4. BL8 setting activated by either MR0[1:0] = 01 and A12 = 0 during READ commands at T4.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable.

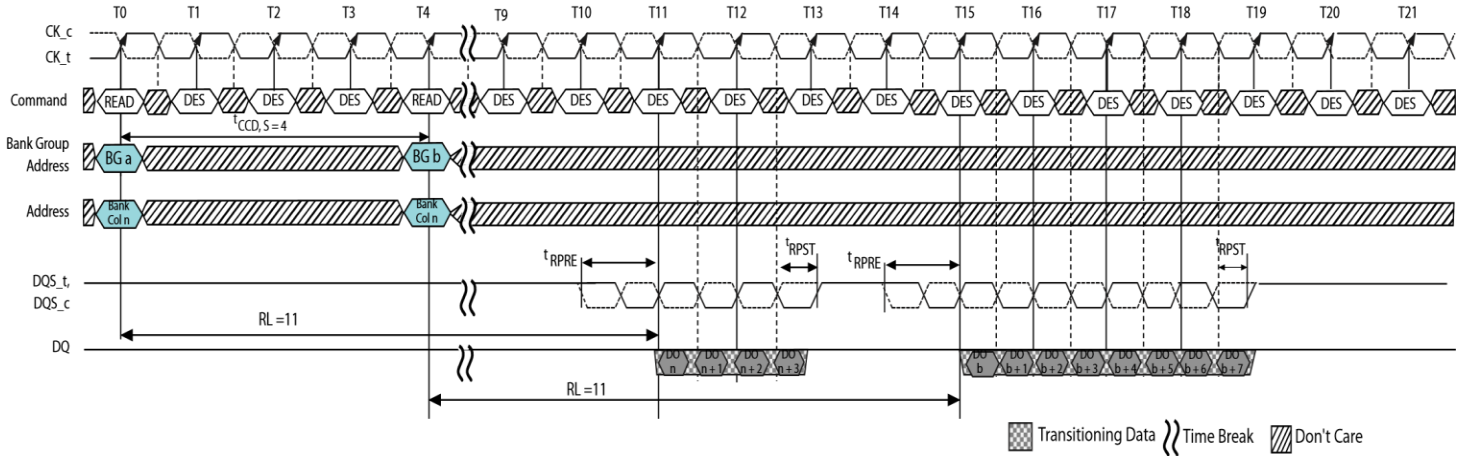

Figure 57 - READ (BC4) to READ (BL8) OTF with 1tCK Preamble in Different Bank Group

Notes:

1. BL = 8, AL = 0, CL = 10, Preamble = 1tCK.
2. DO *n* (or *b*) = data-out from column *n* (or column *b*)
3. DES commands are shown for ease of illustration; other commands may be valid at these times
4. BC4 setting activated by either MR0[1:0] = 01 and A12 = 0 during READ commands at T0.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable.

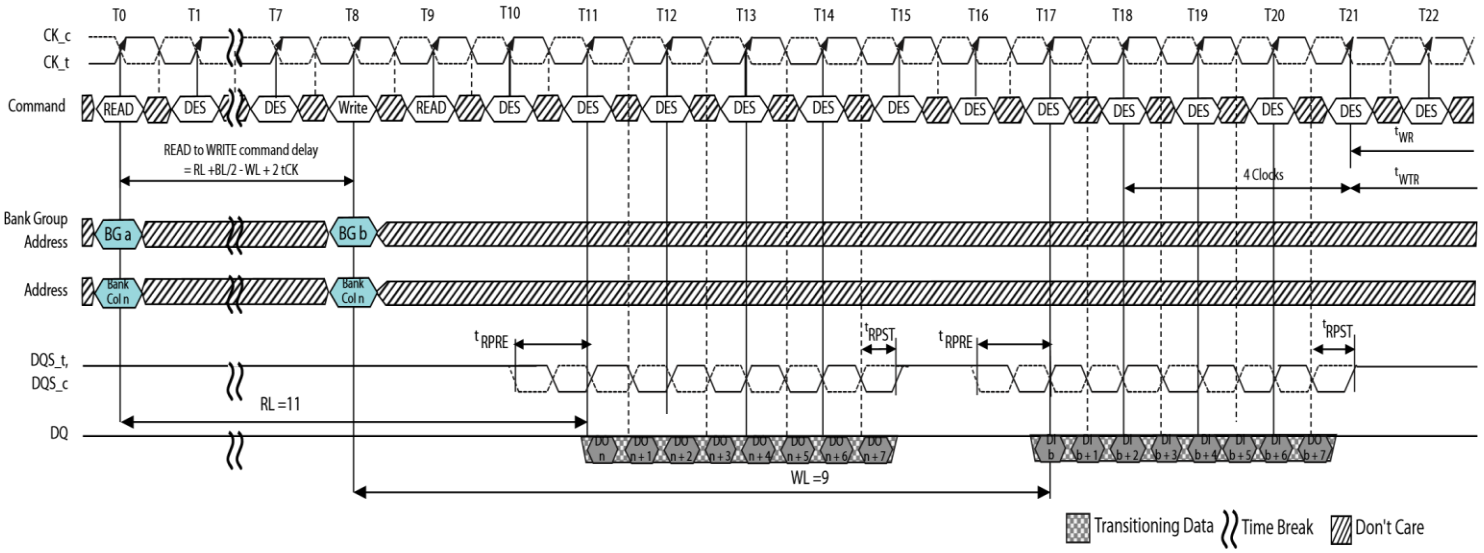

Figure 58 - READ (BL8) to READ (BL8) OTF with 1tCK Preamble in Same or Different Bank Group

Notes:

1. BL = 8, RL = 10 (CL = 10, AL = 0), READPreamble = 1tCK, WL = 9 (CWL = 9, AL = 0), WRITE preamble = 1tCK.
2. DO *n* = data-out from column *n* DI b = data in from column *b*
3. DES commands are shown for ease of illustration; other commands may be valid at these times
4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during READ commands at T8.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

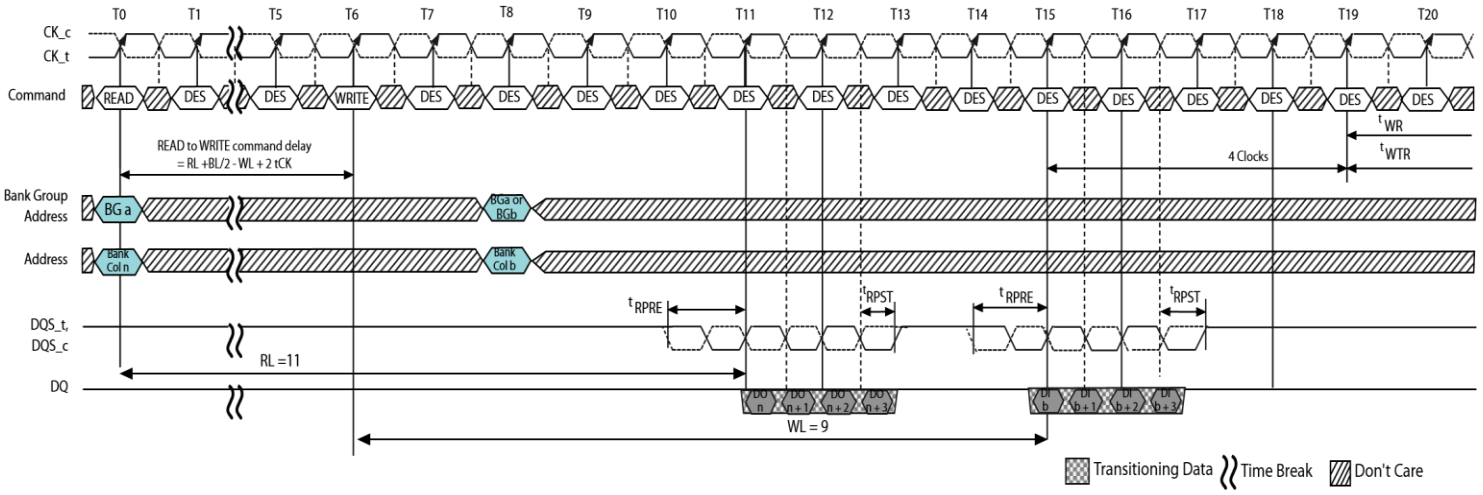

Figure 59 - READ (BC4) OTF to WRITE (BC4) OTF with 1tCK Preamble in Same or Different Bank Group

Notes:

1. BC = 4, RL = 10 (CL = 10, AL = 0), READ Preamble = 1tCK, WL = 9 (CWL = 9, AL = 0), WRITE preamble = 1tCK.
2. DO *n* = data-out from column *n;* DI b = data-in from column *b*
3. DES commands are shown for ease of illustration; other commands may be valid at these times
4. BC4 (OTF) setting activated by either MR0[1:0] = 01 and A12 = 0 during READ commands at T0 and WRITE commands at T6.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write DBI = Disable, Write

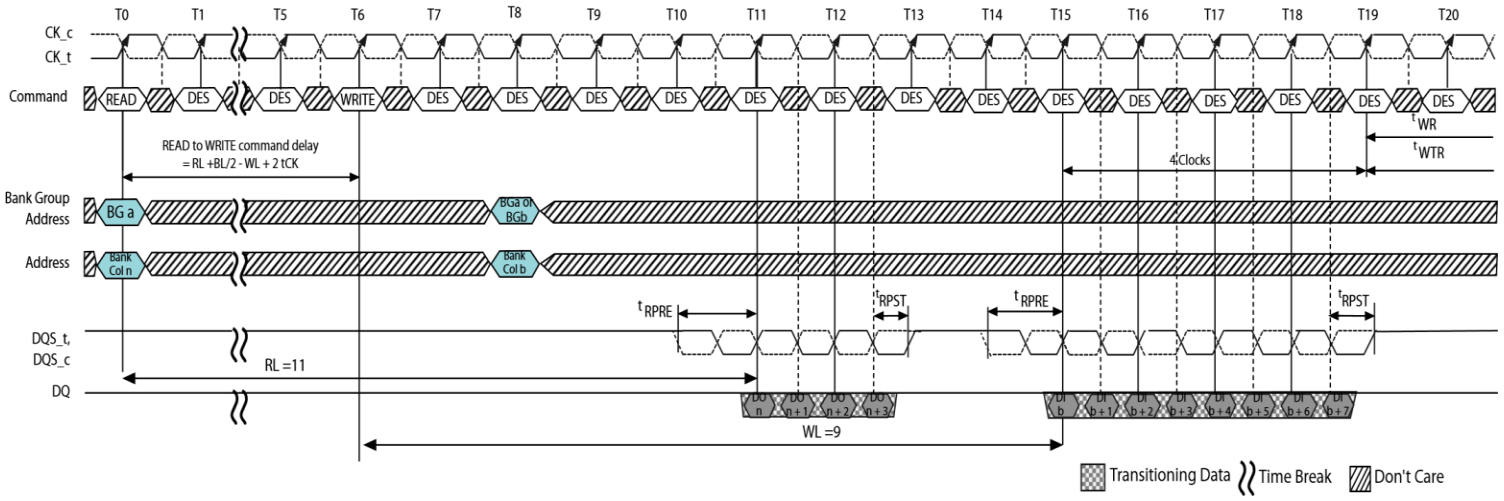

Figure 60 - READ (BC4) Fixed to WRITE (BC4) Fixed with 1tCK Preamble In Same or Different Bank Group

Notes:

1. BC = 4, RL = 10 (CL = 10, AL = 0), READ Preamble = 1tCK, WL = 9 (CWL = 9, AL = 0), WRITE preamble = 1tCK.
2. DO *n* = data-out from column *n;* DI b = data-in from column *b*
3. DES commands are shown for ease of illustration; other commands may be valid at these times
4. BC4 (fixed) setting activated by MR0[1:0] = 01.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

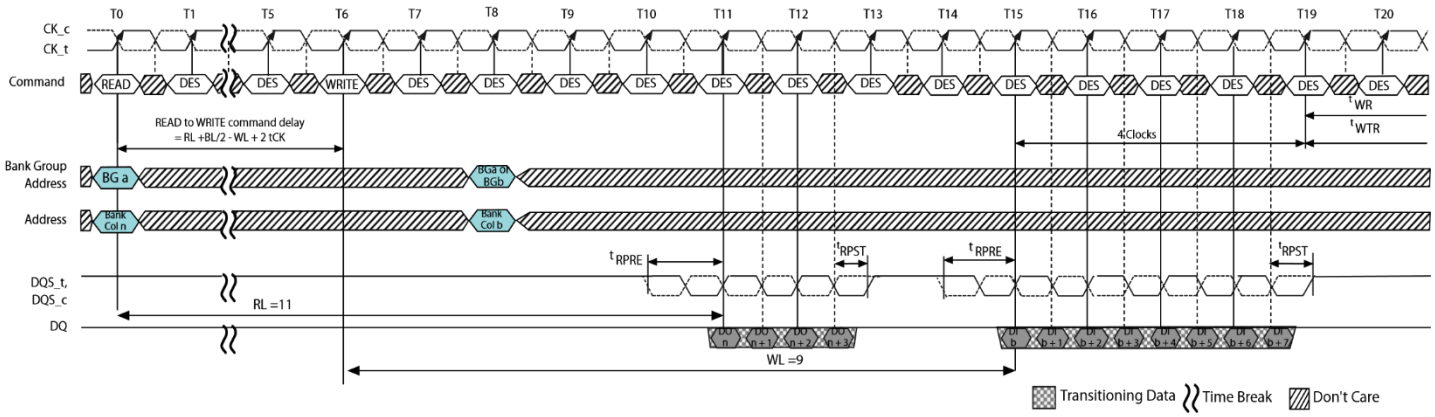

Figure 61 - READ (BC4) to WRITE (BL8) OTF with 1tCK Preamble in Same or Different Bank Group

Notes:

1. BC = 8, RL = 10 (CL = 10, AL = 0), READ Preamble = 1tCK, WL = 9 (CWL = 9, AL = 0), WRITE preamble = 1tCK.
2. DO *n* = data-out from column *n;* DI b = data-in from column *b*
3. DES commands are shown for ease of illustration; other commands may be valid at these times
4. BC4 setting activated by MR0[1:0] = 01 and A12 = 0 during WRITE commands at T0. BL8 setting activated by MR0[1:0] = 01 and A12 = 1 during READ commands at T6.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable. CRC = Disable.

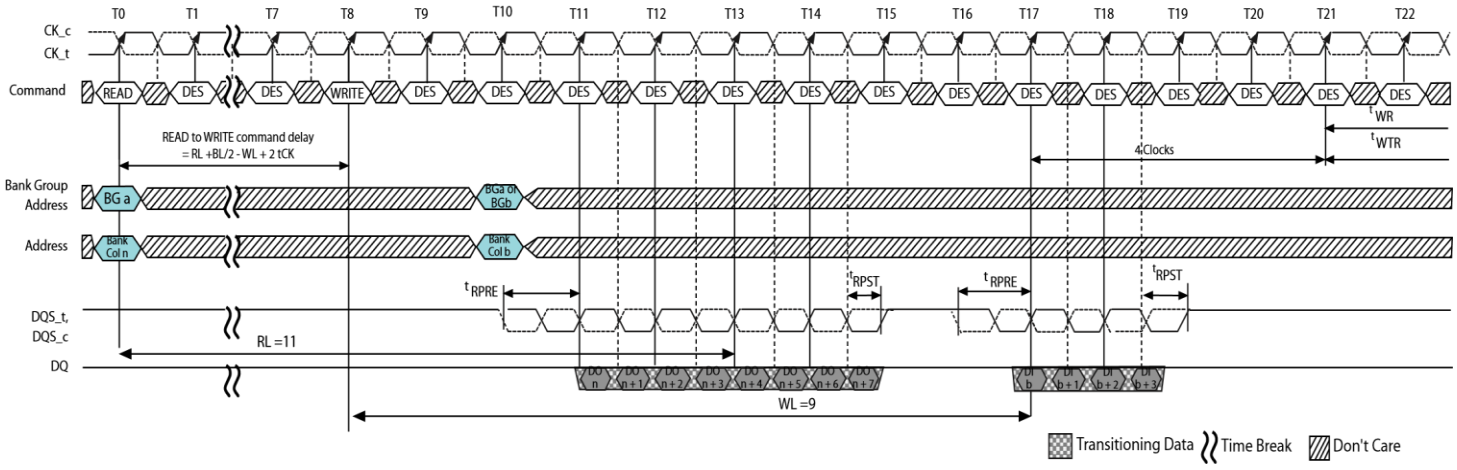

Figure 62 - READ (BL8) to WRITE (BC4) OTF with 1tCK Preamble in Same or Different Bank Group

Notes:

1. BL = 8, RL = 10 (CL = 10, AL = 0), READ Preamble = 1tCK, WL = 9 (CWL = 9, AL = 0), WRITE preamble = 1tCK.
2. DO *n* = data-out from column *n;* DI b = data-in from column *b*
3. DES commands are shown for ease of illustration; other commands may be valid at these times
4. BL8 setting activated by MR0[1:0] = 01 and A12 = 1 during READ commands at T0. BC4 setting activated by MR0[1:0] = 01 and A12 = 0 during READ commands at T8.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

12.22.5.1 READ Operation Followed by a PRECHARGE Operation

The minimum external READ command to PRECHARGE command spacing to the same bank is equal to tRTP with tRTP being the internal READ command to PRECHARGE command delay. Note that the minimum ACT to PRE timing, tRAS, must be satisfied as well. The minimum value for the internal READ command to PRECHARGE command delay is given by tRTP (MIN) = MAX (4 × nCK, 7.5ns). A new bank ACTIVATE command may be issued to the same bank if the following two conditions are satisfied simultaneously:

- The minimum RAS precharge time (tRP [MIN]) has been satisfied from the clock at which the precharge begins.
- The minimum RAS cycle time (tRC [MIN]) from the previous bank activation has been satisfied.

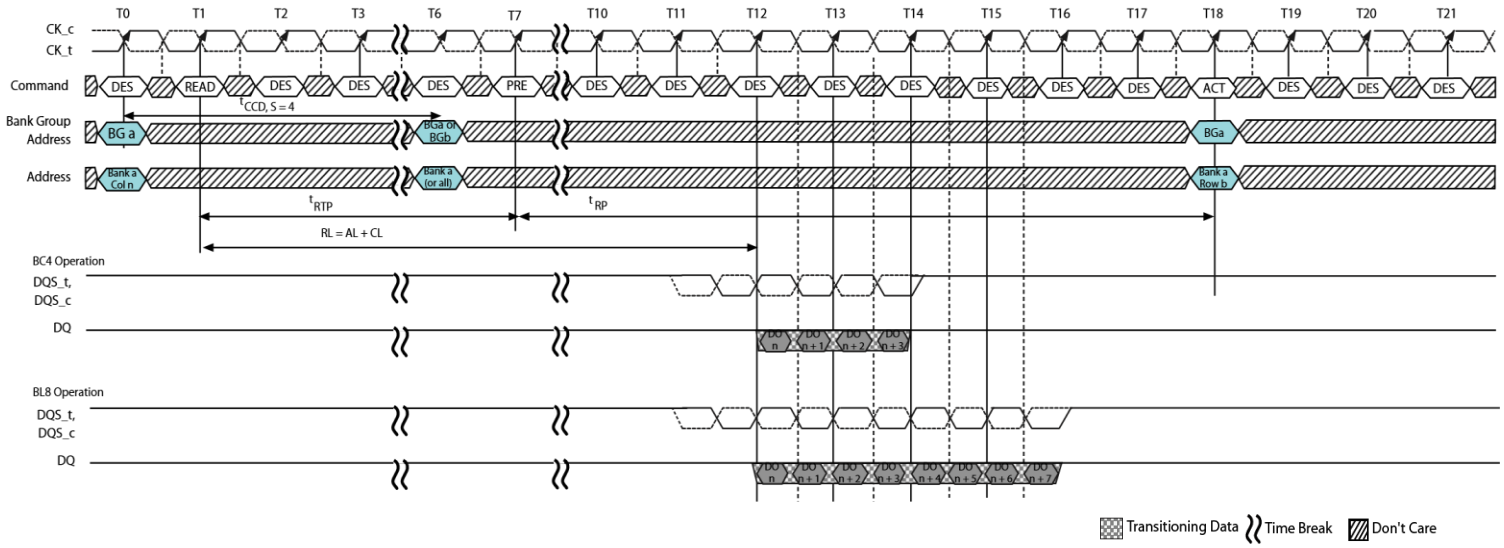

Figure 63 - READ to PRECHARGE with 1tCK Preamble

Notes:

1. RL = 10 (CL = 10, AL = 0), READ Preamble = 1tCK, tRTP = 6, tRP = 11.
2. DO *n* = data-out from column *n.*
3. DES commands are shown for ease of illustration; other commands may be valid at these times
4. The example assumes that tRAS (MIN) is satisfied at the PRECHARGE command time (T7).
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable.

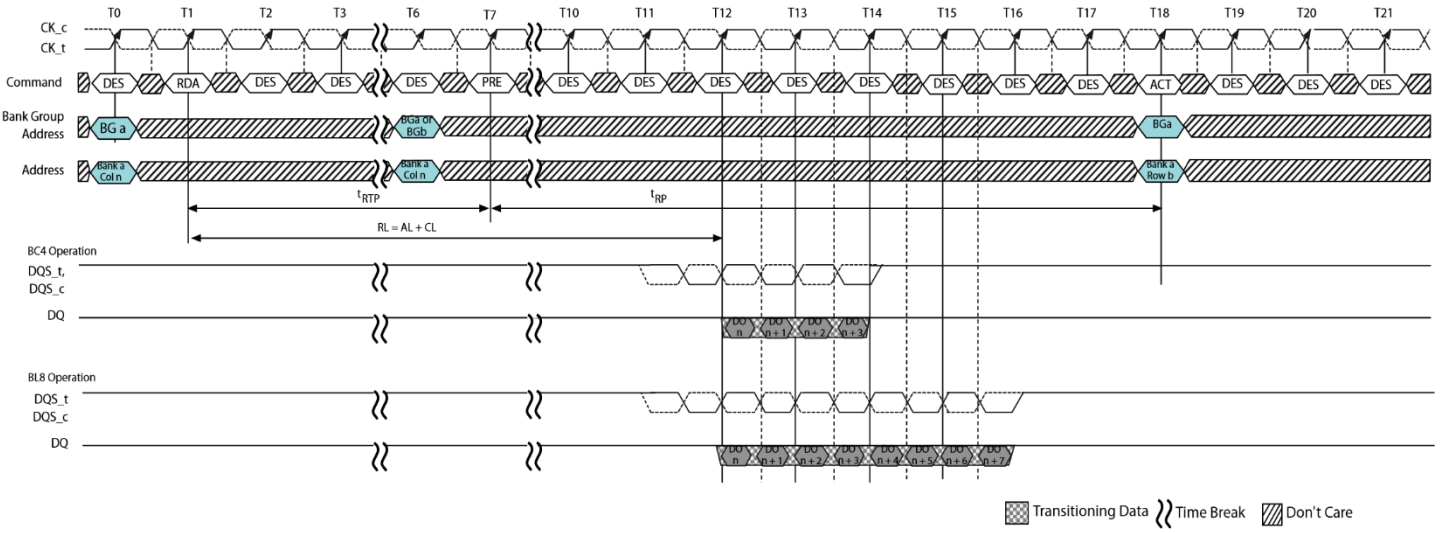

Figure 64 - READ with Auto PRECHARGE and 1tCK Preamble

Notes:

1. RL = 10 (CL = 10, AL = 0), Preamble = 1tCK, tRTP = 6, tRP = 11.
2. DO *n* = data-out from column *n.*
3. DES commands are shown for ease of illustration; other commands may be valid at these times
4. tRTP = 6 setting activated by MR0[A11:9 = 001].
5. This example assumes that tRC (MIN) is satisfied athe the next ACTIVATE command time (T18).
6. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable.

12.23 WRITE Operation

12.23.1.1 WRITE Timing Definitions

The write timings shown in the following figures are applicable in normal operation mode, that is when the DLL is enabled and locked.

12.23.1.2 WRITE Timing - Clock-to-Data Strobe Relationship

The clock-to-data strobe relationship is shown below and is applicable in normal operation mode, that is, when the DLL is enabled and locked.

Rising data strobe edge parameters:

- tDQSS (MIN) to tDQSS (MAX) describes the allowed range for a rising data strobe edge relative to CK.
- tDQSS is the actual position of a rising strobe edge relative to CK.
- tDQSH describes the data strobe high pulse width.
- tWPST strobe going to HIGH, nondrive level (shown in the postamble section of the graphic below). Falling data strobe edge parameters:

- tDQSL describes the data strobe low pulse width.
- tWPRE strobe going to LOW, initial drive level (shown in the preamble section of the graphic below).

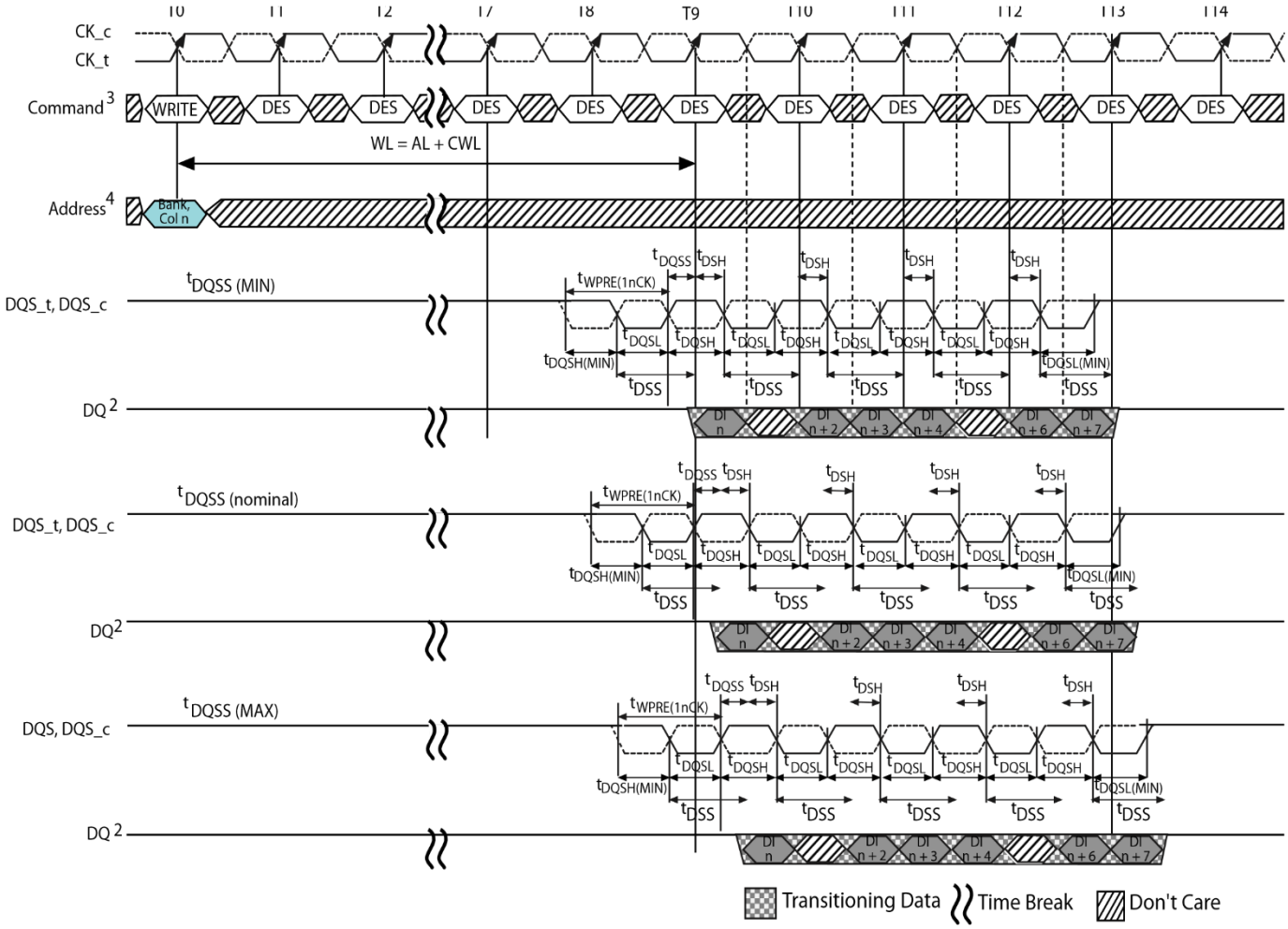

Figure 65 - WRITE Timing Definition

Notes:

1. BL8, WL = 9 (AL = 0, CWL = 9).
2. D_{IN} *n* = data-in from column *n.*
3. DES commands are shown for ease of illustration; other commands may be valid at these times
4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during WRITE command at T0.
5. tDQSS must be met at each rising clock edge.

12.23.1.3 WRITE Timing - Data Strobe-to-Data Relationship

The DQ input receiver uses a compliance mask (Rx) for voltage and timing as shown in the figure below. The receiver mask (Rx mask) defines the area where the input signal must not

encroach in order for the STTMRAM input receiver to be able to successfully capture a valid input signal. The Rx mask is not the valid dataeye. TdiVW and VdiVW define the absolute maximum Rx mask.

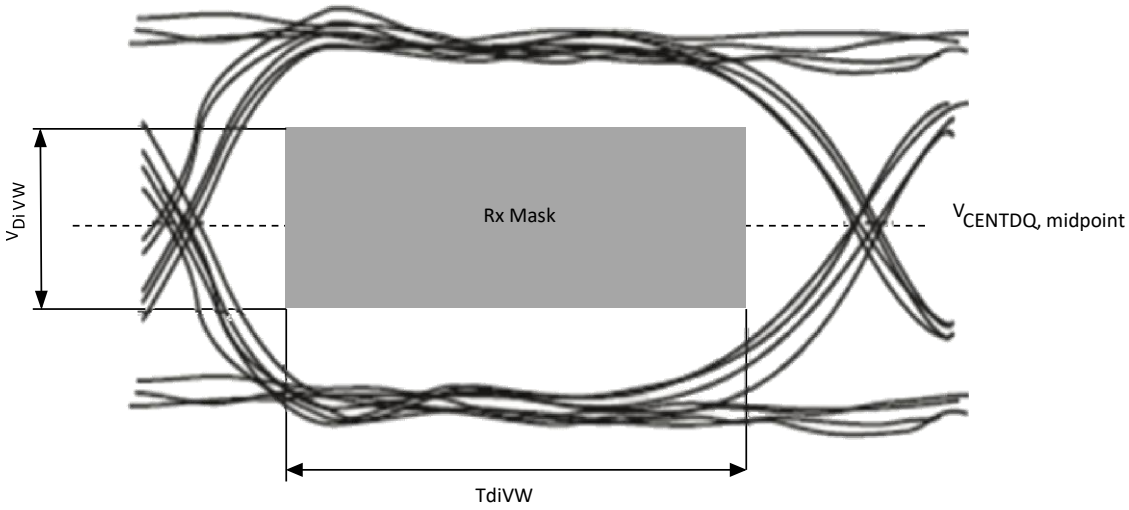

Figure 66 - Compliance Mask

V_{CENTDQ}, midpoint is defined as the midpoint between the largest V_{REFDQ} voltage level and the smallest V_{REFDQ} voltage level across all DQ pins for a given device. Each DQ pin's V_{REFDQ} is defined by the center (widest opening) of the cumulative data input eye as depicted in the following figure. This means a device's level variation is accounted for within the device's Rx mask. The device's V_{REFDQ} level will be set by the system to account for R_{ON} and ODT settings.

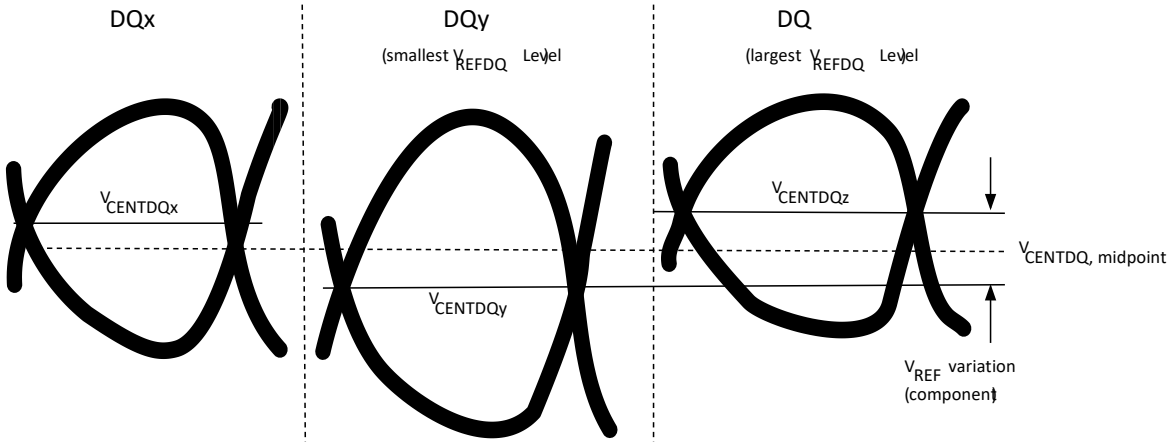

Figure 67 - VCENTDQ, VREFDQ Voltage Variation

The following figure shows the Rx mask requirements both from a midpoint-to-midpoint reference (left side) and from an edge-to-edge reference. The intent is not to add any new requirement or specification between the two but rather how to convert the relationship between the two methodologies. The minimum data-eye shown in the composite view is not actually obtainable due to the minimum pulse width requirement.

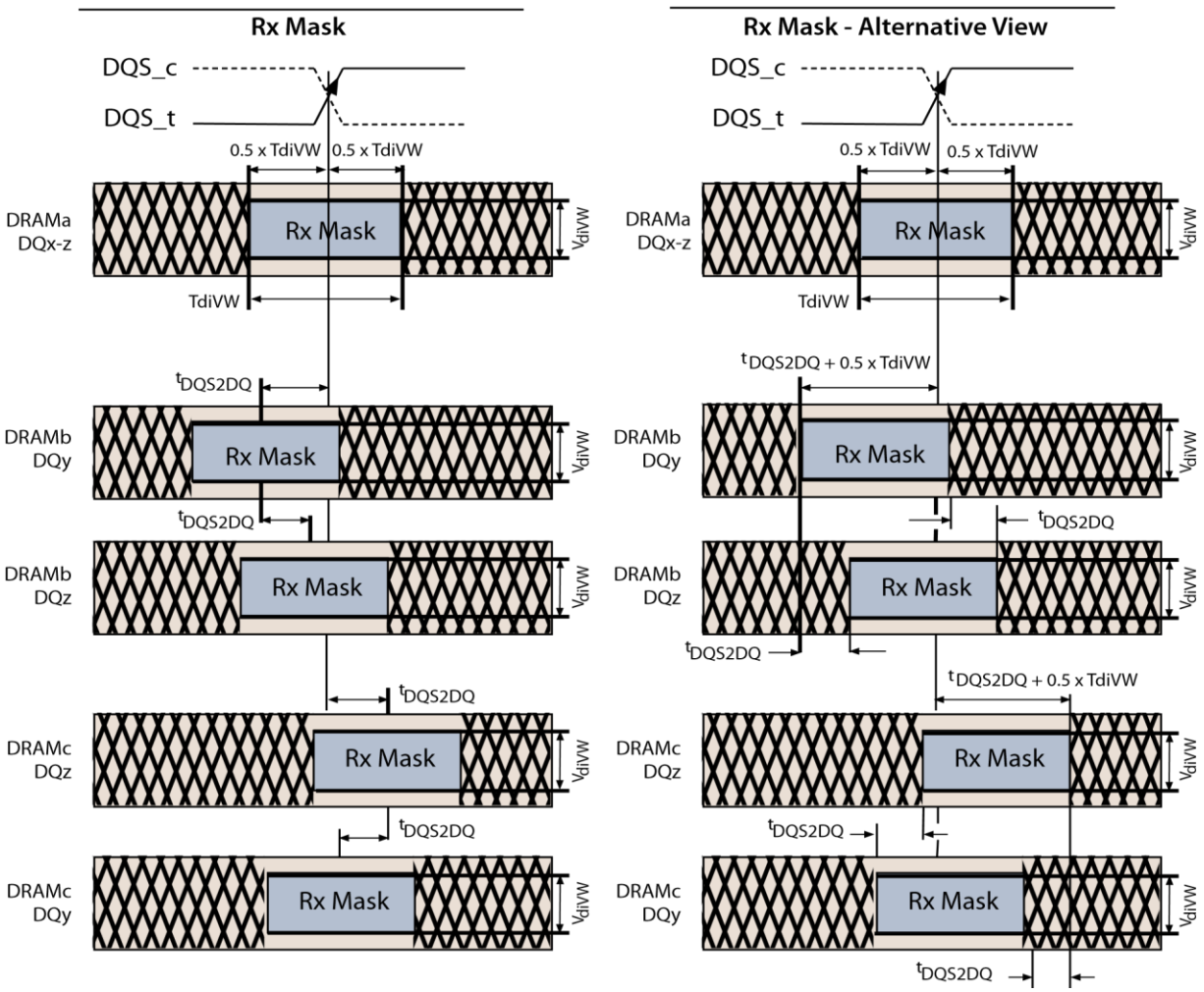

Figure 68 - Rx Mask DQ-to-DQS Timings

Notes:

1. DRAMa represents a DRAM without any DQS/DQ skews.
2. DRAMb represents a DRAM with early skews (negative tDQS2DQ).
3. DRAMc represents a DRAM with delayed skews (positive tDQS2DQ).
4. This figure shows the skew allowed between DRAM-to-DRAM and between DQ-to-DQ for a DRAM. Signals assume data is center-aligned at DRAM latch. TdiPW is not shown; composite data-eyes shown would violat TdiPW.
5. $V_{CENTDQ.midpoint}$ is not shown but is assumed to be midpoint of V_{diVW}.

The previous figure shows the basic Rx mask requirements. Converting the Rx mask requirements to a classical DQ-to-DQS relationship is shown in the following figure. It should become apparent that the ST-DDR4 write training is required to take full advantage of the Rx mask.

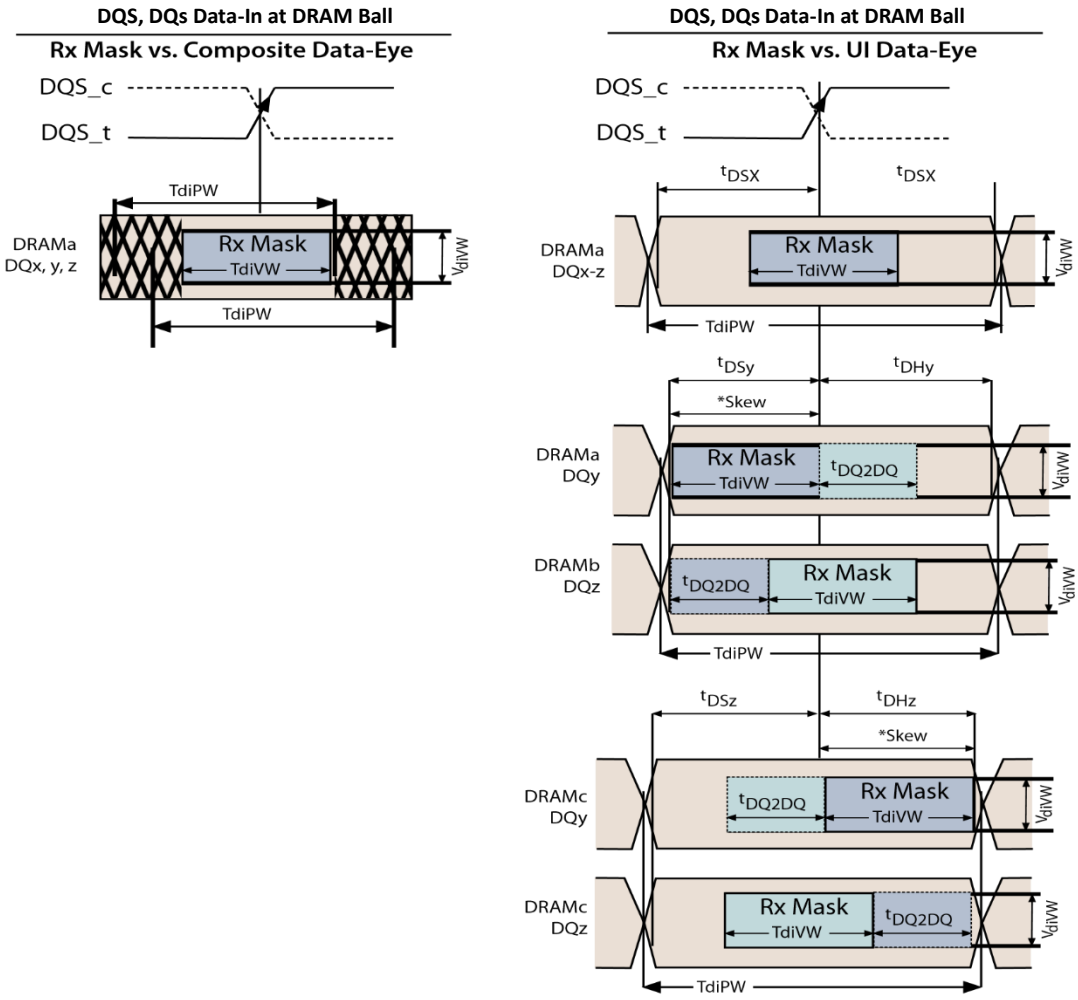

Figure 69 - Rx Mask DQ-to-DQS MRAM-Based Timings

Notes:

1. DQx represents an optimally centered mask. DQy represents earliest valid mask. DQz represents latest valid mask.
2. *Skew - tDQSDQ + 0.5 x TdiVW
3. DRAMa represents a DRAM without any DQS/DQ skews.
4. DRAMb represents a DRAM with early skews (negative tDQS2DQ, tDQSy > *Skew).
5. DRAMc represents a DRAM with delayed skews (positive tDQS2DQ, tDQHZ > *Skew).
6. tDS/tDH are traditional data-eye setup/hold edges at DC levels.
7. tDS and tDH are not specified; tDH and tDS may be any value provided the pulse width and Rx mask limits are not violated tDH (MIN) > TdiVW + tDS (MIN) + tDQ2DQ

The ST-DDR4 device input receivers are expected to capture the input data with an Rx mask of TdiVW provided the minimum pulse width is satisfied. The ST-DDR4 controller will have to train

the data input buffer to utilize the Rx mask specifications to this maximum benefit. If the ST-DDR4 controller does not train the data input buffers, then the worst case limits have to be used for the Rx mask (TdiVW + 2 × tDQS2DQ), which will generally be the be the classical minimum (tDS and tDH) and is required as well.

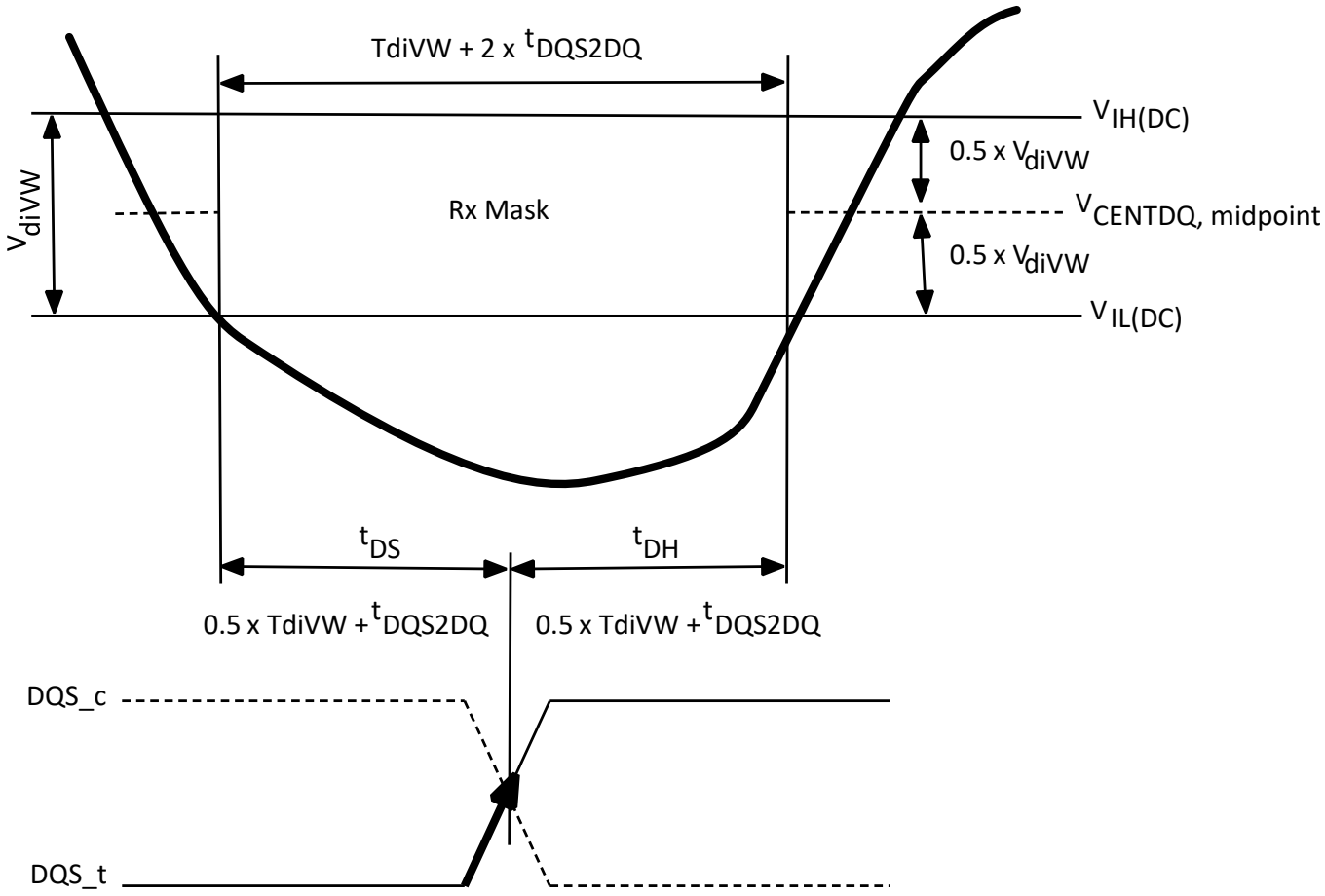

Figure 70 - Example of Data Input Requirements Without Training

12.23.2 WRITE Burst Operation

The following write timing diagrams are intended to help understand each write parameter's meaning and are only examples. Each parameter will be defined in detail separately. In these write timing diagrams, CK and DQS are shown aligned, and DQS and DQ are shown center-aligned for the purpose of illustration.

DDR4 WRITE command supports bursts of BL8 (fixed), BC4 (fixed), and BL8/BC4 on-the-fly (OTF); OTF uses address A12 to control OTF when OTF is enabled:

- A12 = 0, BC4 (BC4 = burst chop)
- A12 = 1, BL8

WRITE commands can issue precharge automatically with a WRITE with auto precharge (WRA) command, which is enabled by A10 HIGH.

- WRITE command with A10 = 0 (WR) performs standard write, bank remains active after WRITE burst

WRITE command with A10 = 1 (WRA) performs write with auto precharge, bank goes into precharge after WRITE burst

The DATA MASK (DM) function is supported for the x8 and x16 configurations. The DM function shares a common pin with the DBI_n and TDQS functions. The DM function only applies to WRITE operations and cannot be enabled at the same time the DBI function is enabled.

- If DM_n is sampled LOW on a given byte lane, the device masks the write data received on the DQ inputs. If DM_n is sampled HIGH on a given byte lane, the device does not mask the data and writes this data into the device's core.
- If CRC write is enabled, then DM enabled (via MRS) will be selected between write CRC nonpersistent mode (DM disabled) and write CRC persistent mode (DM enabled).

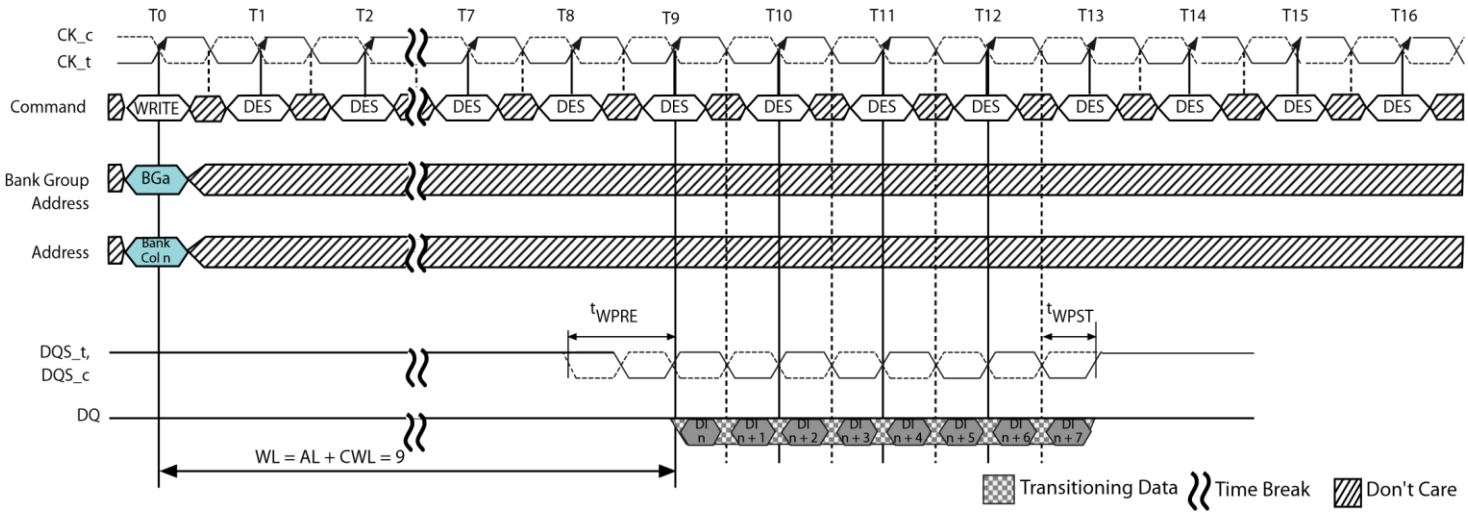

Figure 71 - WRITE Burst Operation, WL=9 (CWL=9, BL8)

Notes:

1. BL8, WL = 0, AL = 0, CWL = 9, Preamble = 1tCK.
2. DI *n* = data-in from column *n.*
3. DES commands are shown for ease of illustration; other commands may be valid at these times
4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during WRITE command at T0.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable.

12.24 WRITE Operation Followed by Another WRITE Operation

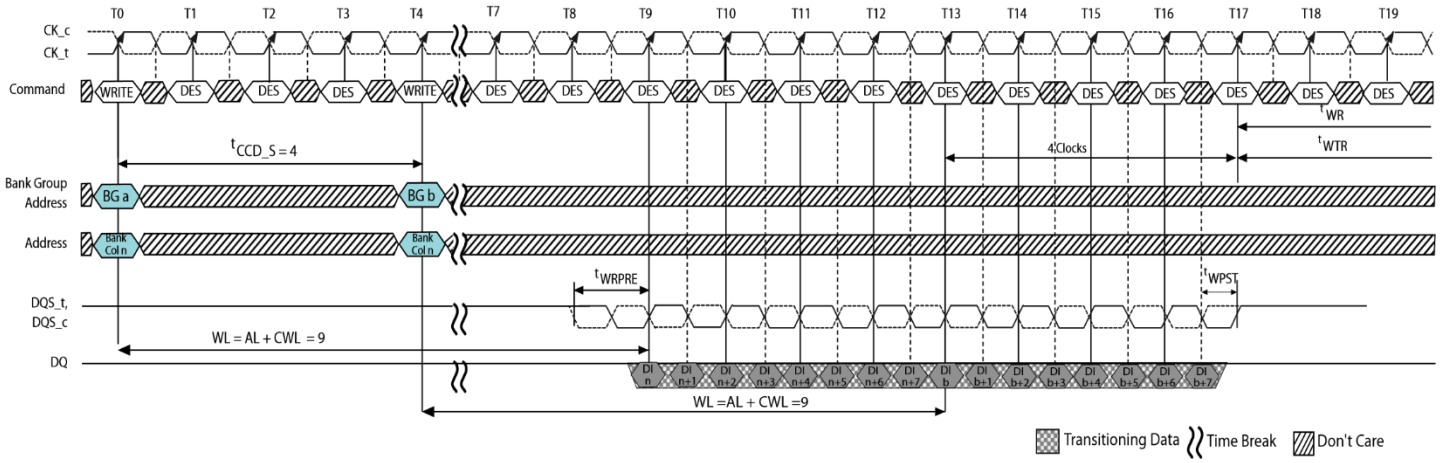

Figure 72 - Consecutive WRITE (BL8) with 1tCK Preamble in Different Bank Group

Notes:

1. BL8, AL = 0, CWL = 9, Preamble = 1tCK.
2. DI *n* (or *b*)= data-in from column *n* (or column *b*).
3. DES commands are shown for ease of illustration; other commands may be valid at these times
4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during WRITE command at T0 and T4.
5. CA parity = Disable, CS to CA latency = Disable, Write DBI = Disable, Read DBI = Disable.
6. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T17.

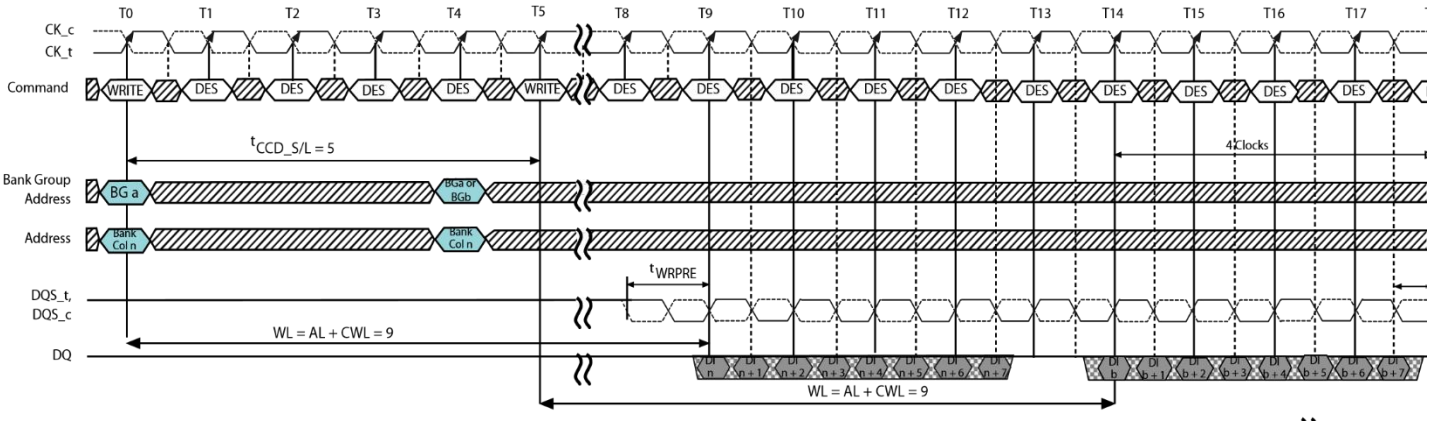

Figure 73 - Non-Consecutive WRITE (BL8) with 1tCK Preamble in Same of Different Bank Group

Notes:

1. BL8, AL = 0, CWL = 9, Preamble = 1tCK, tCCD_S/L = 5tCK.
2. DI *n* (or *b*)= data-in from column *n* (or column *b*).
3. DES commands are shown for ease of illustration; other commands may be valid at these times
4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during WRITE command at T0 and T5.
5. CA parity = Disable, CS to CA latency = Disable, Write DBI = Disable, Write CRC = Disable.
6. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T18.

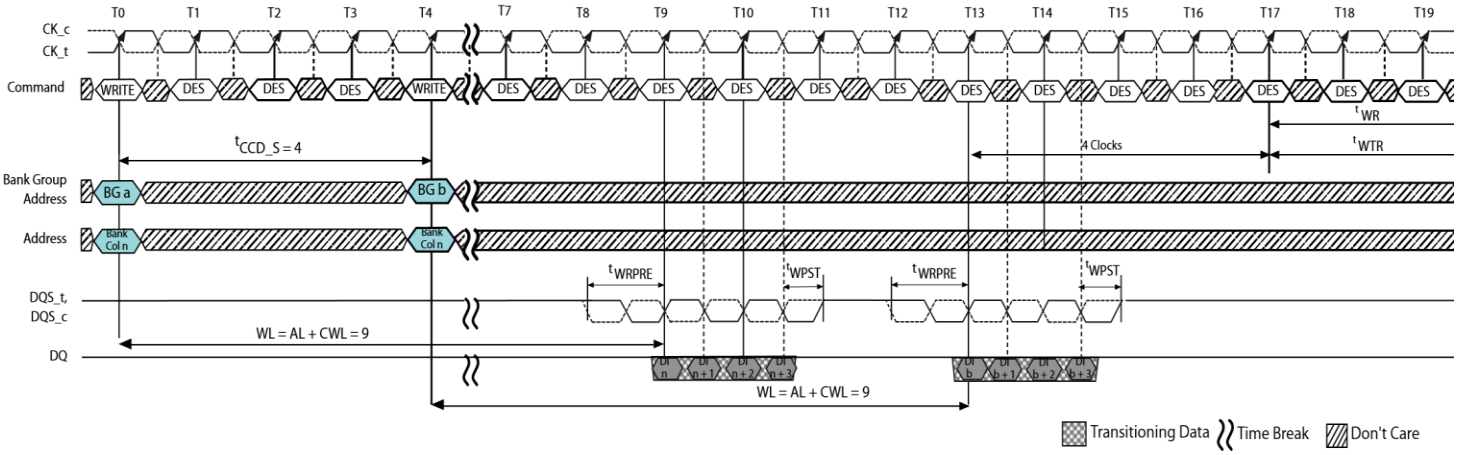

Figure 74 - WRITE (BC4) OTF to WRITE (BC4) OTF with 1tCK Preamble in Different Bank Group

Notes:

1. BC4, AL = 0, CWL = 9, Preamble = 1tCK.
2. DI *n* (or *b*)= data-in from column *n* (or column *b*).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by either MR0[1:0] = 01 and A12 = 0 during WRITE command at T0 and T4.
5. CA parity = Disable, CS to CA latency = Disable, Write DBI = Disable, Write CRC = Disable.
6. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T17.

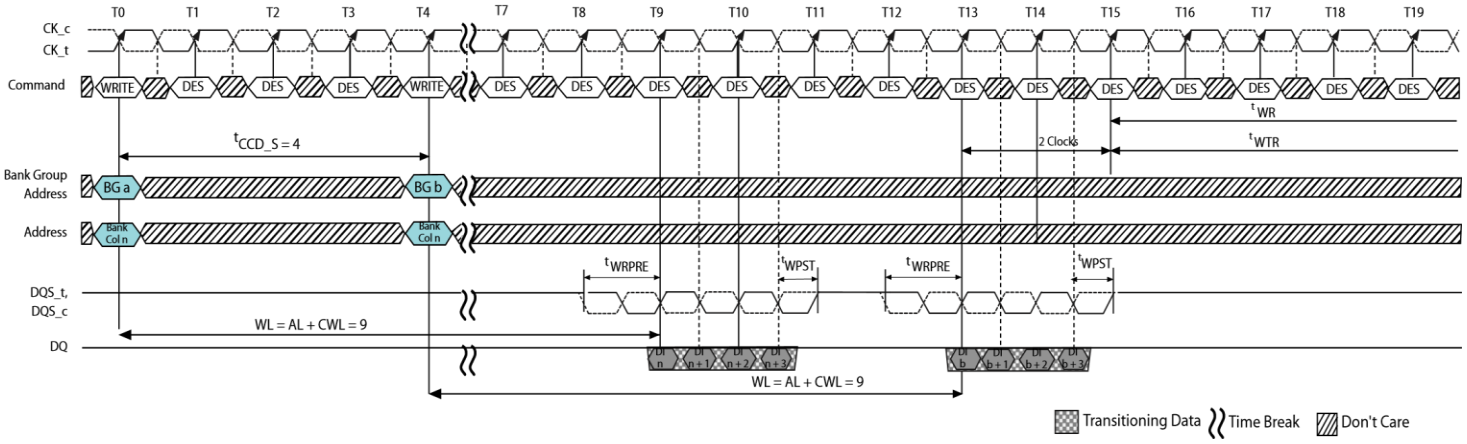

Figure 75 - WRITE (BC4) Fixed to READ (BC4) Fixed with 1tCK Preamble in Same Bank Group

Notes:

1. BC4, AL = 0, CWL = 9, Preamble = 1tCK.
2. DI *n* (or *b*)= data-in from column *n* (or column *b*).
3. DES commands are shown for ease of illustration; other commands may be valid at these times
4. BC4 setting activated by either MR0[1:0] = 10.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.
6. The write recovery time (tWTR_L) is referenced from the first rising clock edge after the last write data shown at T11.

12.24.1.1 WRITE Operation Followed by PRECHARGE Operation

The minimum external WRITE command to PRECHARGE command spacing is equal to WL (CWL) plus 4tCK (BL8/BC4-OTF) plus tWR. The minimum ACT to PRE timing, tRAS, must be satisfied as well.

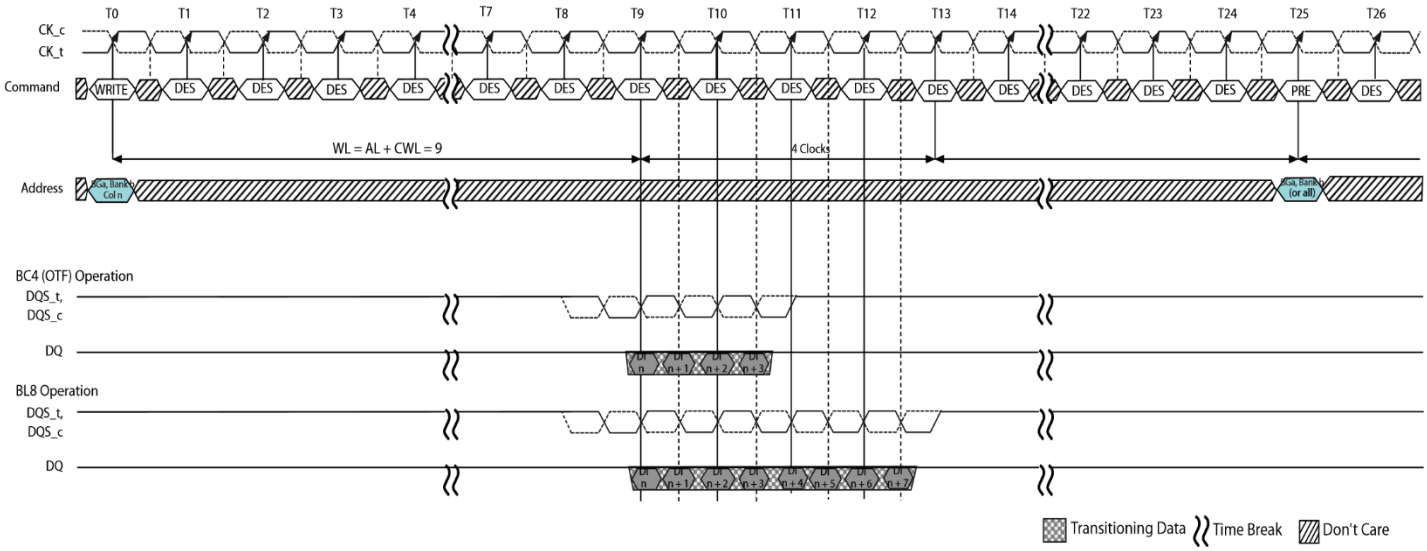

Figure 76 - WRITE (BL8/BC4-OTF) to PRECHARGE with 1tCK Preamble

Notes:

1. BL = 8 with BC4-OTF, WL = 9 (CWL = 9, AL = 0), Preamble = 1tCK tWR = 12.
2. DI *n* (or *b*)= data-in from column *n* (or column *b*).
3. DES commands are shown for ease of illustration; other commands may be valid at these times
4. BC4 setting activated by either MR0[1:0] = 01 and A12 = 0 during WRITE command at T0. BL8 setting activated by MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during WRITE command at T0.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write CRC = Disable.
6. The write recovery time (tWR) is referenced from the first rising clock edge after the last write data shown at T13. tWR specifies the last burst WRITE cycle until the PRECHARGE command can be issued to the same bank.

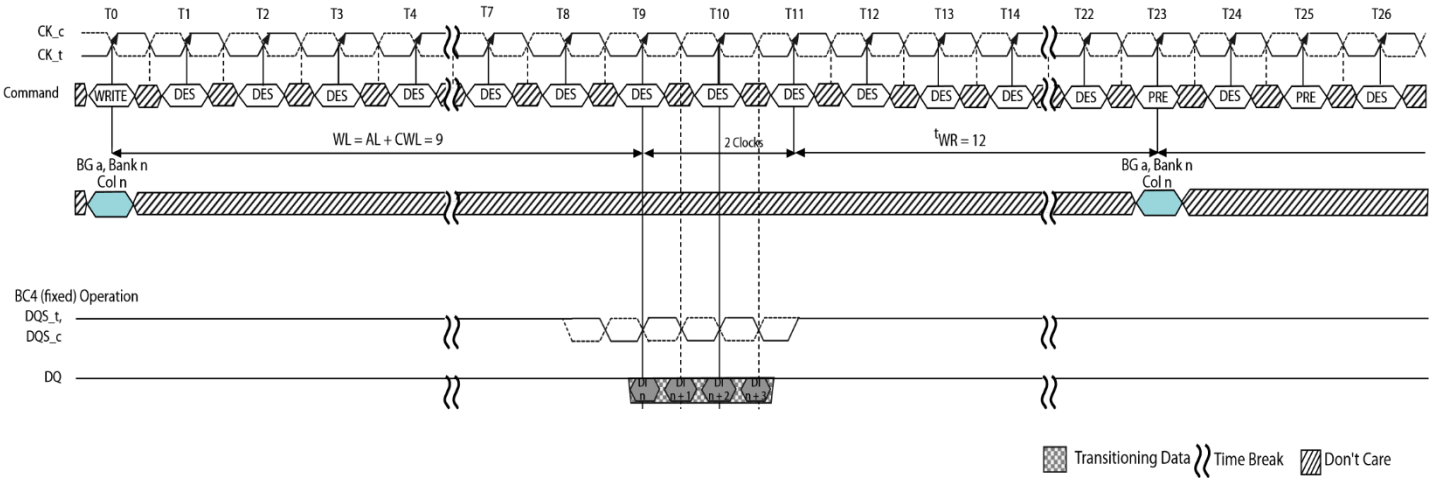

Figure 77 - WRITE (BC4-Fixed) to PRECHARGE with 1tCK Preamble

Notes:

1. BC4 = fixed, WL = 9 (CWL = 9, AL = 0), Preamble = 1tCK tWR = 12.
2. DI *n* = data-in from column *n.*
3. DES commands are shown for ease of illustration; other commands may be valid at these times
4. BC4 setting activated by MR0[1:0] = 10.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write CRC = Disable.
6. The write recovery time (tWR) is referenced from the first rising clock edge after the last write data shown at T11.
   tWR specifies the last burst WRITE cycle until the PRECHARGE command can be issued to the same bank.

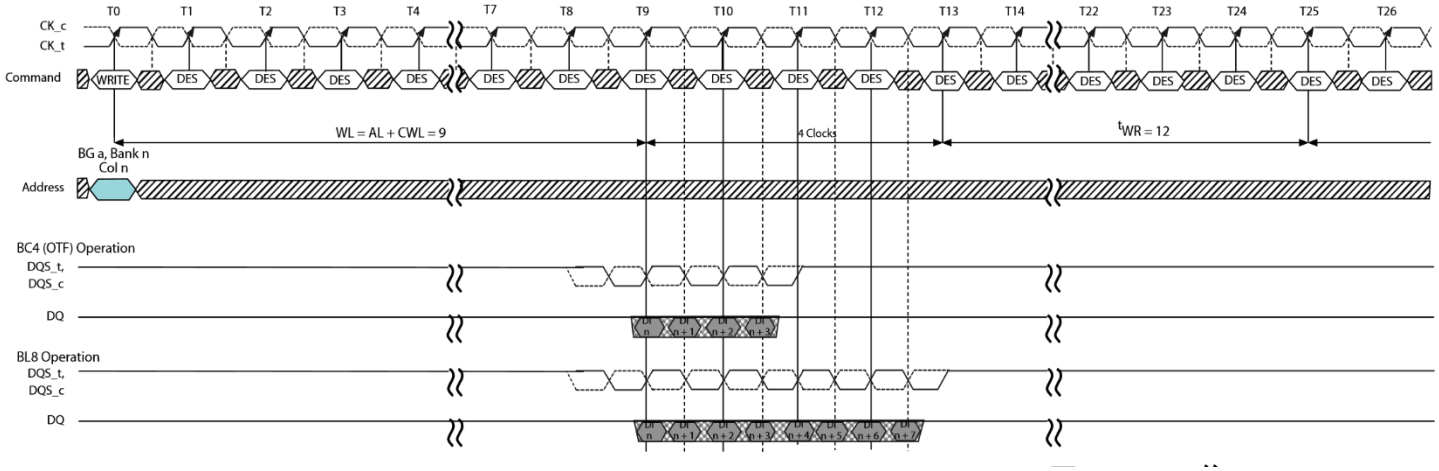

Figure 78 - WRITE (BL8/BC4-OTF) to Auto PRECHARGE with 1tCK Preamble

Notes:

1. BL = 8 with BC4-OTF, WL = 9 (CWL = 9, AL = 0), Preamble = 1tCK tWR = 12.
2. DI *n* = data-in from column *n.*
3. DES commands are shown for ease of illustration; other commands may be valid at these times
4. BC4 setting activated by MR0[1:0] = 01 and A12 = 0 during WRITE command at T0. BL8 setting activated by MR0[1:0] = 00 or MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during WRITE command at T0.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write CRC = Disable.
6. The write recovery time (tWR) is referenced from the first rising clock edge after the last write data shown at T13.
   tWR specifies the last burst WRITE cycle until the PRECHARGE command can be issued to the same bank.

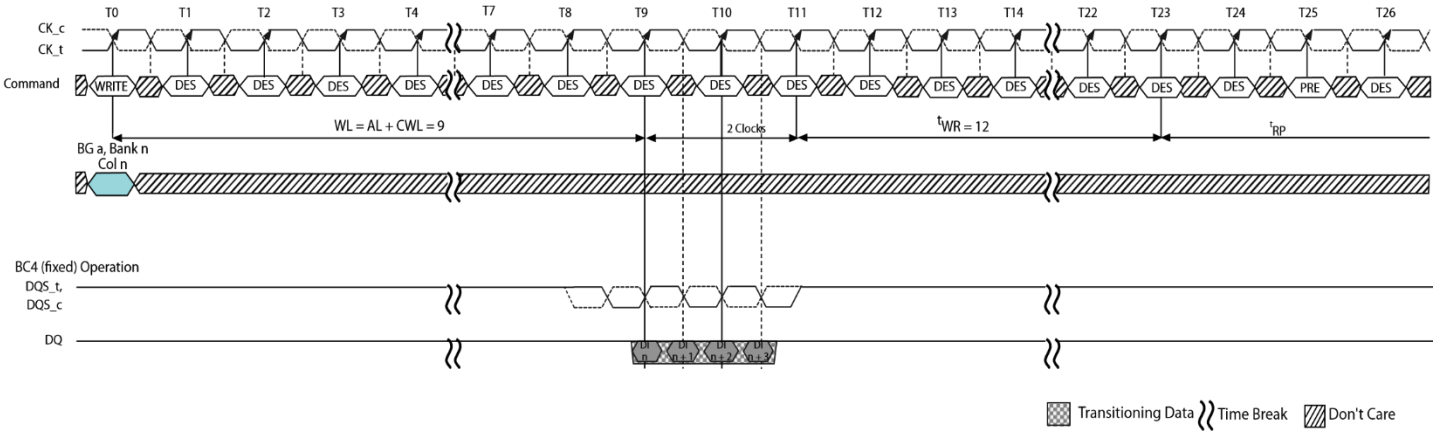

Figure 79 - WRITE (BC4-Fixed) to Auto PRECHARGE with 1tCK Preamble

Notes:

1. BC4 = fixed, WL = 9 (CWL = 9, AL = 0), Preamble = 1tCK tWR = 12.
2. DI *n* = data-in from column *n.*
3. DES commands are shown for ease of illustration; other commands may be valid at these times
4. BC4 setting activated by MR0[1:0] = 10.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, CRC = Disable.
6. The write recovery time (tWR) is referenced from the first rising clock edge after the last write data shown at T11.
   tWR specifies the last burst WRITE cycle until the PRECHARGE command can be issued to the same bank.

12.25 ZQ Calibration Commands

A ZQ CALIBRATION command is used to calibrate the device's R_{ON} and ODT values. The device needs a longer time to calibrate the output driver and on-die termination circuits at initialization. The ZQCS command is not supported and will be ignored.

The ZQCL command is used to perform the initial calibration during the power-up initialization sequence. This command may be issued at any time by the controller depending on the system environment. The ZQCL command triggers the calibration engine inside the ST-DDR4 device and, after calibration is achieved, the calibrated values are transferred from the calibration engine to device's I/O, which is reflected as an updated output driver and ODT values.

The first ZQCL command issued after reset is allowed a timing period of tZQinit to perform the full calibration and the transfer of values. All other ZQCL commands except the first ZQCL command issued after reset are allowed a timing period of tZQoper.

ZQ CALIBRATION commands can also be issued in parallel to DLL lock time when coming out of self-refresh. Upon self-refresh exit, the device will not perform an I/O calibration without an explicit ZQ CALIBRATION command. The earliest possible time for a ZQ CALIBRATION command (long only) after self-refresh exit is tXSF.

In systems that share the ZQ resistor between devices, the controller must not allow any overlap of tZQoper, or tZQinit between the devices.

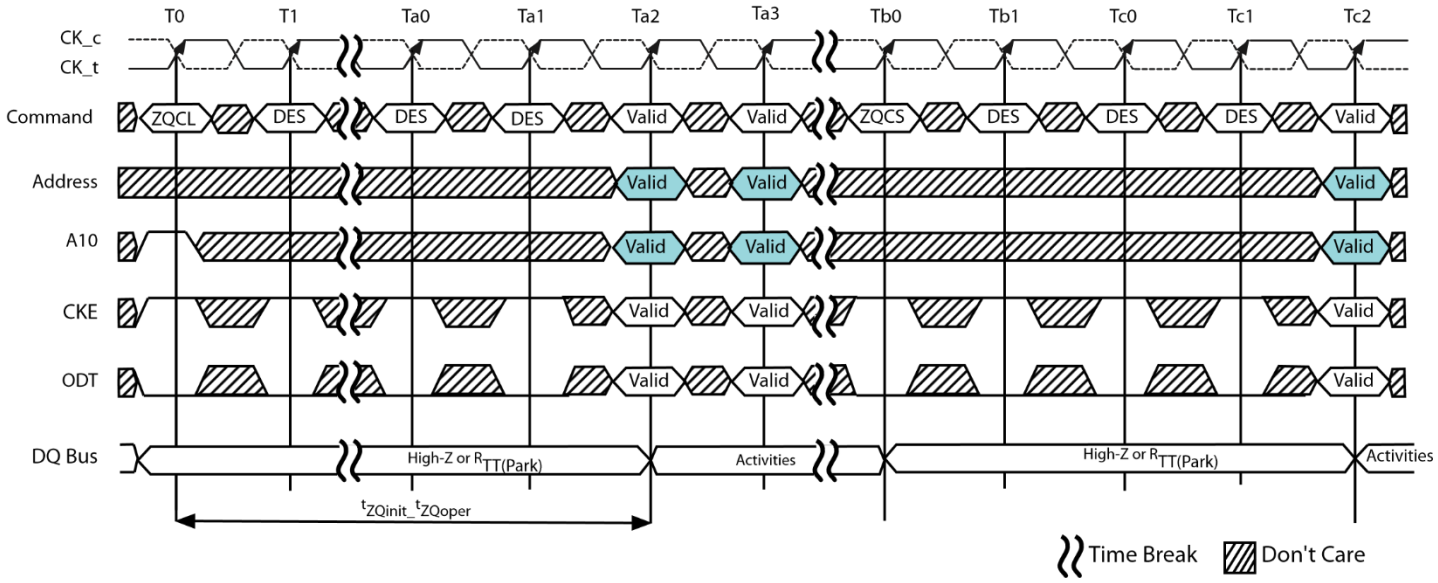

Figure 80 - ZQ Calibration Timing

Notes:

1. CKE must be continuously registered HIGH during the calibration procedure.
2. On-die termination must be disabled via ODT signal or MRS during the calibration procedure or the DRAM will automatically disable $R_{TT}1$.
3. All devices connected to the DQ bus should be High-Z during the calibration procedure.

12.26 On-Die Termination

On-die termination (ODT) is a feature that enables the device to change termination resistance for each DQ, DQS, and DM_n signal (and TDQS when enabled via MR1[11]=1) by setting an $R_{TT(park)}$ value in MR5[8:6]. Only $R_{TT(Park)}$ is supported on this device.

The ODT feature is turned off and not supported in self-refresh mode.

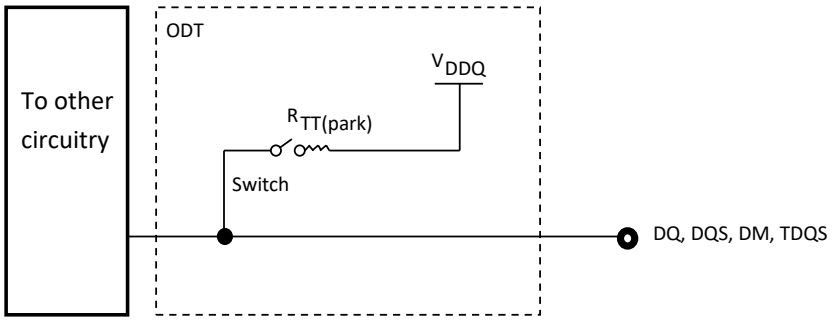

Figure 81 - Functional Representation of ODT

The switch is enabled by the internal ODT control logic, which uses the external ODT pin and other control information. The value of $R_{TT(park)}$ is determined by settings mode register bits MR5[8:6] = 000 – 111 (See Mode Register 5). The ODT pin will be ignored if the mode register MR1 is programmed to disable $R_{TT(NOM)}$, MR1[10:8] = 000 and in Self-Refresh mode.

Note: RTT(park) and "ODT termination disabled" are the only supported ODT modes.

13. ORDERABLE PART NUMBERS (OPN)

Table 70 - Orderable Part Numbers

Org	Temp	Package	Speed Bin	Shipping Container	Part Number
128Mb x 8	0 - 85°C	10x13mm 78-ball BGA	1333	Tray	EMD4E001G08G1-150CAS2
				Tape and Reel	EMD4E001G08G1-150CAS2R
64Mb x 16	0 - 85°C	10x13mm 96-ball BGA	1333	Tray	EMD4E001G16G2-150CAS2
				Tape and Reel	EMD4E001G16G2-150CAS2R

13.1 Orderable Part Number (OPN) Decoder

Table 71 – Orderable Part Number Example, documents how each part number field describes a specific attribute or feature of the ST-DDR4 MRAM device. The example part number will be EMD4E001G08G1-150CAS2, which is an ST-DDR4 MRAM, 1Gb density, 1333MT/s speed, x8 device shipping to the customer in trays and it will be an Engineering Sample (ES). For Tape & Reel, the OPN, MPN and CPN on the shipping label will have the letter "R" appended to the end of each part number.

Table 71 – Orderable Part Number Example
EMD4E001G08G1-150CAS2

	Vendor	Category	Family	Voltage	Density	IO Width	Package	Timing	Temp	Revision	Class	Packing
Example Orderable Part Number	E	M	D4	E	001G	16	G2	-150	C	A	S2	
Everspin E												
STT-MRAM M												
DDR4 D4												
Vdd and Vddq = 1.2V E												
1Gb 001G												
x8 08 x16 16												
78-Ball BGA 10mm x 13mm G1 96-Ball BGA 10mm x 13mm G2												
fCK=667Mhz (1333MT/s) -150												
Commercial[1] C												
Device Version A												
Device Class S2												
Tray <blank> Tape & Reel R												

[1] Commercial Toper = 0 - 85°C

Notice there will not be a Tray or Tape & Reel designation marked on the parts. The exact orderable part number will be printed on the shipping label. Just below the part number on the drawing in Figure 82 is the assembly date code and grade. In our example, ES is marked on the part to designate an Engineering Sample (ES). For production this field will be left blank[1].

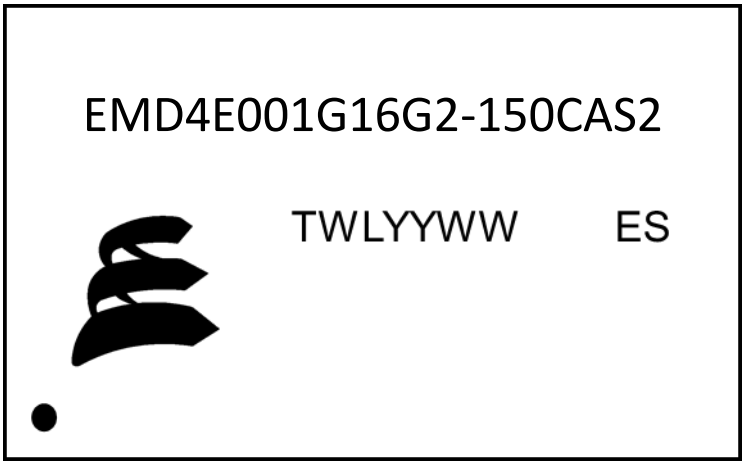

Figure 82 - Part markings showing example OPN

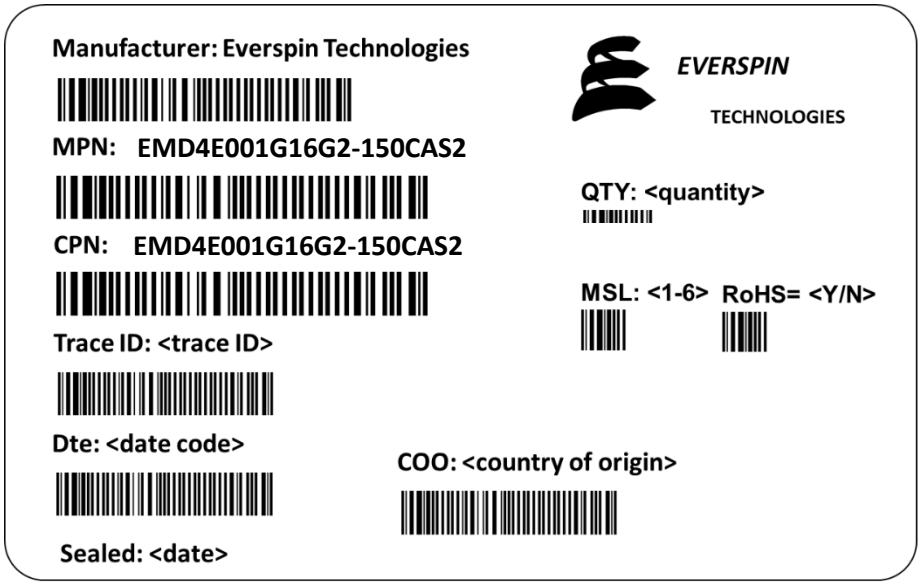

Figure 83- Sample shipping label using example OPN

[1] The graphic depiction of the part markings on page 1 of this document is a graphical design and does not match the part markings as documented in Figure 82 - Part markings showing example OPN.

13.2 PACKAGE OUTLINE DRAWINGS

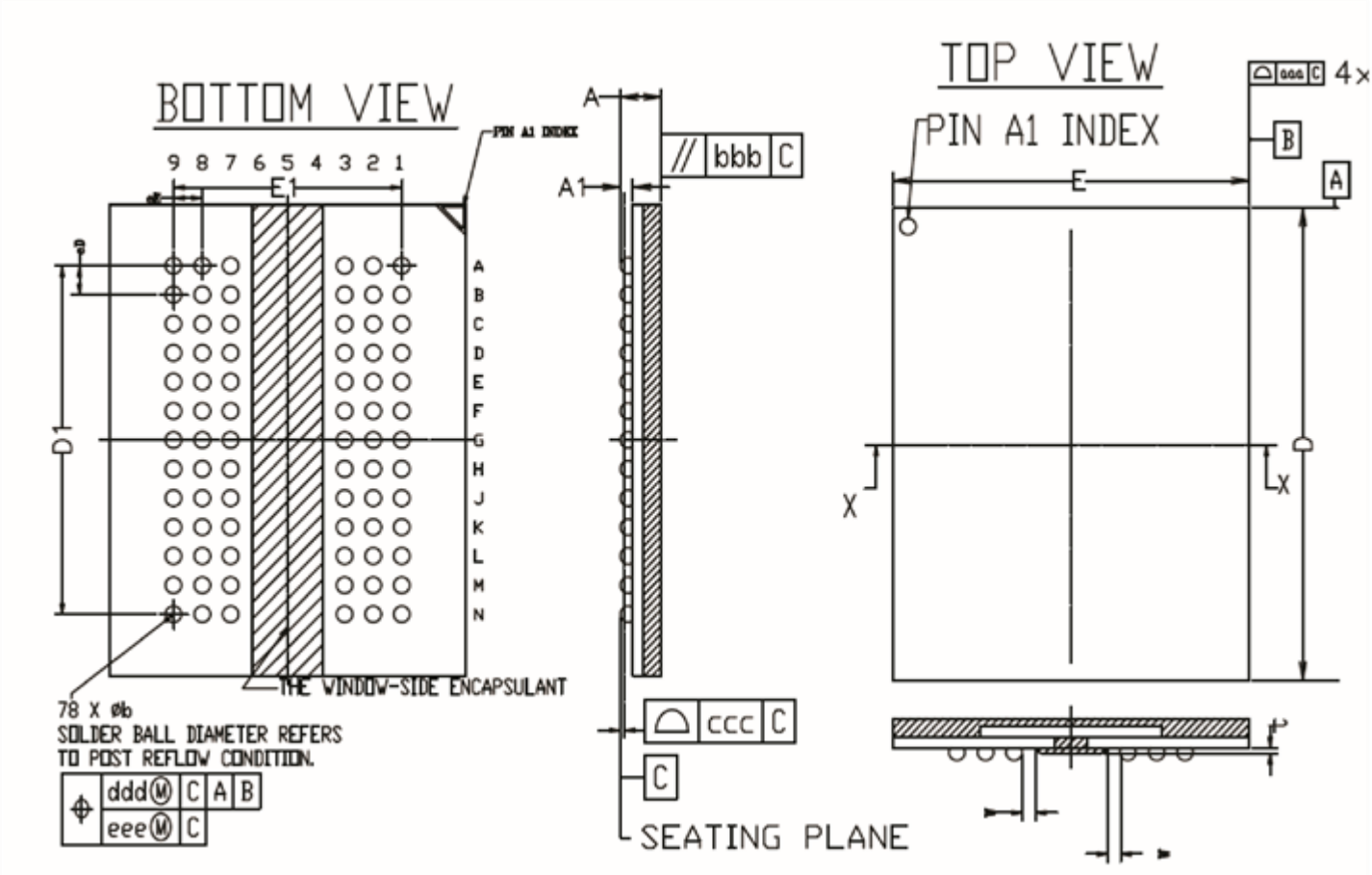

Figure 84 - 78-Ball BGA Package Outline (x8)

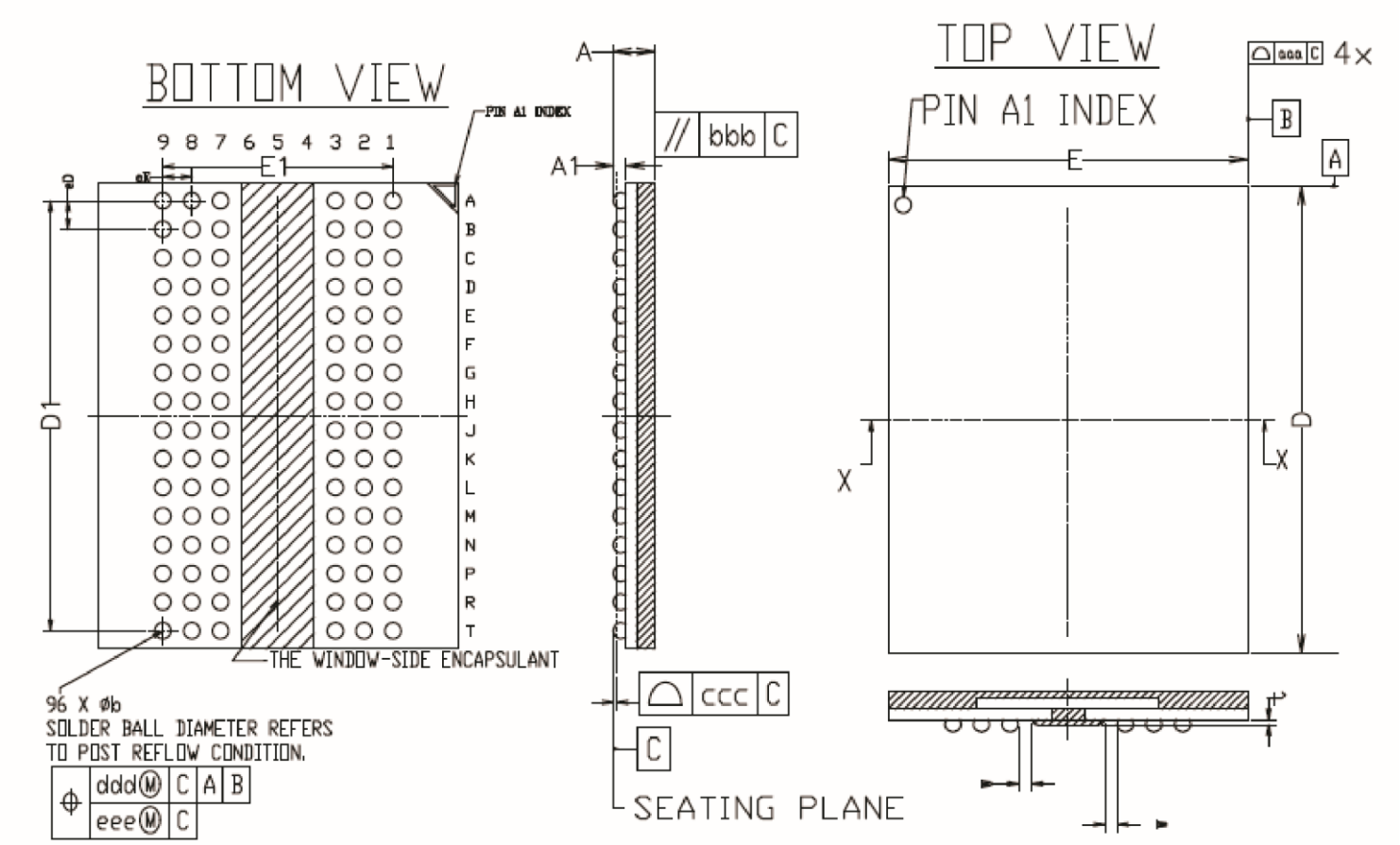

Figure 85 - 96-Ball BGA Package Outline (x16)

Table 72 – 78-ball (x8) & 96-ball (x16) BGA Dimension References (mm)

Reference	Min	Nom	Max
A	-	-	1.20
A1	0.25	-	0.40
b	0.40	-	0.50
D	12.90	13.00	13.10
E	9.90	10.00	10.10
D1 (x8)	9.60 BSC		
D1 (x16)	12.00 BSC		
E1	6.40 BSC		
eE	0.80 BSC		
eD	0.80 BSC		
aaa	-	-	0.15
bbb	-	-	0.20
ccc	-	-	0.10
ddd	-	-	0.15
eee	-	-	0.08
W	0.1	-	-
t	-	-	0.20

Notes:

1. All dimensions are in millimeters.
2. “eE “ and “eD” represent the basic solder ball grid pitch.
3. “b” is measurable at the maximum solder ball diameter parallel to primary datum C. The solder ball diameter is 0.45mm before reflow. The solder ball pad 0.40mm.
4. Primary datum C are defined by the spherical.
5. The overall package thickness “A” already considers collapse.
6. Package dimensions conform to JEDEC MO-207
7. The distance between the top surface of the smallest solder ball (ball height) and window-side encapsulant must be greater than 0.10mm.
8. The height of the window-side encapsulant “t” could vary, but it must always satisfy the requirement of Note 7.
9. “W” defines the distance between the edge of the solder ball and the window-side encapsulant.
10. The only difference between the 78-ball BGA and the 96-ball BGA is dimension D1.

REV	Date	Description of Change
0.6	October 2, 2017	Initial Draft - Preliminary, NDA Required.
0.7	January 24, 2017	Table 8 - 78-ball FBGA x8 (top view) and Table 9 - 96-ball FBGA x16 (top view)- Balls F2, G2, and G8 are changed to NC and Signals C0/CKE1, C1 / CS_n, and C2/ODT1 are deleted. Table 33 – Command and Address Timing, section references to page size deleted. Table 34 – Command and Address Timing with (CL) new spec format for tWTR_L and tWTR_S. Table 33 – Command and Address Timing - Removed “CL” from the Write Recovery Time CL column. ACTIVATE-to-ACTIVATE command [same and different back group] timing for tRRD_S and tRRD_L revised to Min=10ns for all speed bins. Table 40 – Refresh Timing, REFRESH-to-ACTIVATE and Average periodic refresh interval information revised. Note 3 added. Table 40 – Refresh Timing, “tREFI3” replaced with “See Note 3”. Table 41 – Self-Refresh Timing, all tRFC references deleted. Minimum CKE low pulse value revised to tST. Note 2 added. Table 65 – Bank Staggering Time - tST timing revised. Table 64 - DDR4 Bank Group Timings deleted. Following tables renumbered.
0.8	January 26, 2017	Table 15 - tRCD changed to 70ns.
0.92	January 18, 2018	Update document date
0.93	March 23, 2018	Updated table 67 with new part numbers
0.93	August 26, 2018	Removed Dynamic ODT from the product Updated several timing parameters to reflect current product capabilities Updated CWL througout the document to reflect product Figure 41-44 updated to reflect proper timing Updated figure 4 to use tPW_RESET_S
0.96	October 20, 2018	Updated part number Updated timing parameters and associated diagrams
0.98	April 2019	Expanded Table 1 into 3 new tables compromising Enhancements (Table1), Deviations (Table2) and Unsupported features (Table3) from the JESD-7A JEDEC DRAM specification Removed references to MPSM Added “future row address timing numbers” Added simplified state diagram Added simplified architectural block diagram for x8 and x16 devices

REV	Date	Description of Change
		Removed references to the STORE (STO) and STORE ALL (STOA) commands Added REFRESH command section Updated Orderable Part Numbers section Added part marking figure and example shipping label Added IDD Test Patterns and Test Conditions to obtain proper Current values Added separate Table of Contents, List of Tables, and List of Figures Added current values for IDD0 – IDD7 Added embedded links for Table of Contents and List of Tables Updated stale references Added place holder for Data Retention graph
0.99	Sept 2019	Update S2 timing parameters
1.0	Oct 2019	Updated data retention specification Updated table 65 to remove “default” comment
1.1	Feb 2020	Page 1 Features: Data retention 3 months at 70C Table 5 Data Retention 3 months@70C Table 11 Maximum Operating Case Temperature 85 Table 71 updated to reflect S2 OPN Added RoHS logo on page 1
1.2	August 2020	Added NC ball/signal name to Table 10. Corrected Figs. 82 and 83. Update Table 19 for IDD0, IDD1, IDD7. Description of cycle endurance in Table 5 clarified. Removed *Preliminary* from Page 1.
1.3	October 2022	Updated Table 27 to correct data pattern for IDD7 measurement. Removed footnote on Table 70, OPN. Updated Suite in company address. Corrected Table 3, Fine Granularity Refresh Mode, MR3 bit settings.

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