Replacing the Cypress CY14V256LA-BA35 nvSRAM with Everspin's MR256D08BMA45 MRAM

GENERAL CONSIDERATIONS for REPLACING nvSRAM with MRAM

Every write with an Everspin MRAM is instantly non-volatile for at least 20 years. There is no transfer of data from a volatile to a non-volatile memory cell, no external capacitors or back up batteries. The elimination of external components, highly reliable data retention, and 45ns SRAM compatible READ/WRITE Access times make the Everspin MRAM a viable candidate for replacing the Cypress CY14V256LA-BA35 nvSRAM without compromising system performance.

EVERSPIN MRAM MEMORY

Everspin is the global leader in commercially viable MRAM technology and Everspin MRAM products are present in hundreds of applications demanding high-speed, reliable, non-volatile memory.

MR256D08B COMPARISON TO CY14V256LA

The Everspin MRAM solution provides:

- Always Non-Volatile. No Unreliable Capacitor Dependent Backup Cycles
- No V_{CAP} or V_{BATT} required
- Immediate (<1ns) Power-off with no loss of data
- No complex Software STORE/RECALL routines
- Fast Start-up time (2ms vs. 20ms)
- Unlimited Read and Write cycles - No Wear-out Concerns
- 20-Year Data Retention with No Cycling Dependence
- Fewer components means smaller design footprint and lower total BOM cost
- Directly replaces the Cypress nvSRAM
- 45ns MRAM vs. 35ns nvSRAM

COMPATIBILITY

The Everspin MR256D08BMA45 (48 BGA) MRAM is pin compatible with the Cypress CY14V256LA-BA35

TIMING COMPATIBILITY

Both Everspin MRAM and nvSRAM have compatible asynchronous SRAM timing. The MRAM however, retains data even at power off for an indefinite period of time and over temperature cycling. The nvSRAM has 35ns read/write cycle time vs. 45ns access time for the MRAM.

It is important to note that the Everspin MR256D08BMA45 device requires a minimum of 12ns hold time from Write Enable (and Chip Enable) high to Address invalid (Please see T_{WHAX} and T_{EHAX} in the MR256D08BMA45 data sheet available here.) Most microprocessors can accommodate this Hold time.

PIN COMPATIBILITY

- 256Kb organized in the 32Kx8 configuration
- 3.3 volt nominal operation
- Standard SRAM parallel address pins (A0-14)
- Standard byte-wide, bidirectional data pins (DQ0-7)
- Standard control signals (/E, /W, /G)

The MR256D08B does not require an external capacitor and the other associated passive components required by the CY14V256LA-BA35 devices.

The primary differences between the Cypress and Everspin devices are the two I/O's on the nvSRAM labeled: V_{CAP} and /HSB. These I/O's are used to support the nvSRAM backup cycle and are not required for operation of the MRAM.

V_{CAP} pin
A capacitor is required on the V_{CAP} I/O (Ball E3) on nvSRAM devices. Everspin assigns a "Do not connect" (DC) to the corresponding pins on the MRAM. When replacing the Cypress nvSRAM with the Everspin MRAM, it is recommended that this I/O be either left floating or kept at V_{SS}. If a capacitor or V_{DD} is connected to this pin, it will have no effect on MRAM operation. However, the device may draw more current than if this pin is pulled to V_{SS} or left floating.

/HSB pin
The /HSB I/O of the nvSRAM (Ball G2) is used to either initiate a Hardware Store or indicate a Hardware Store is in process. The corresponding I/O on the MRAM is labeled as "No connect" (NC), therefore, a host processor should not expect the MRAM to assert this I/O or respond to a change in state of this I/O.
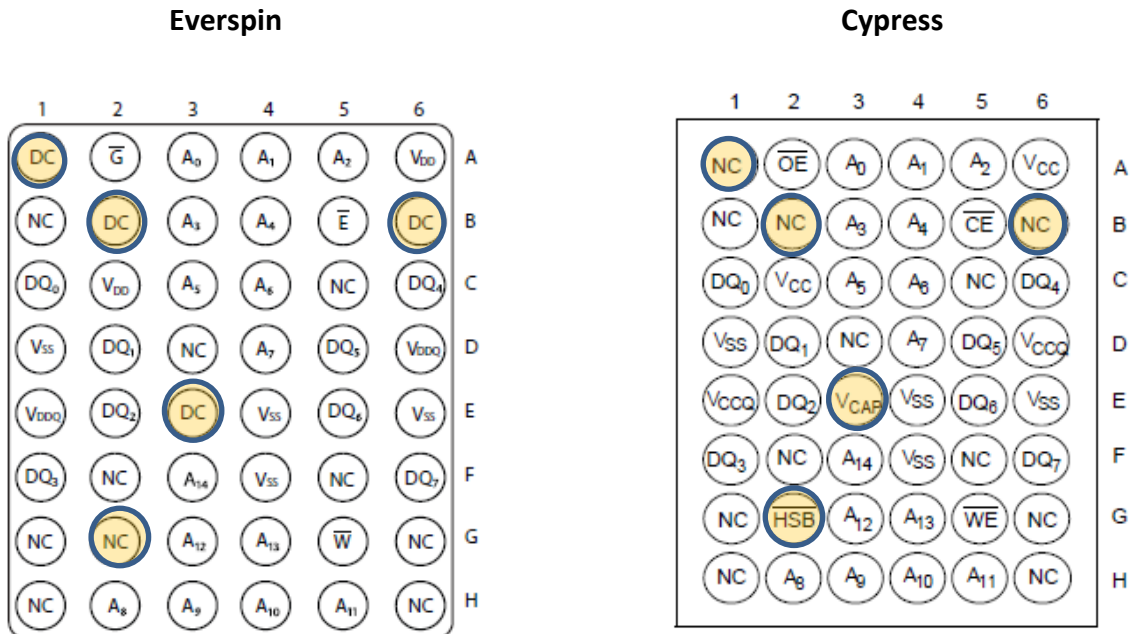
I/O DIFFERENCES

Everspin   **Cypress**

Figure 1 - Pin function comparison between MRAM and nvSRAM, 48 BGA package

PIN #	Everspin	Cypress	Everspin connection	Everspin Comments
A1	DC	NC	Do not connect	Internally pulled down. Prefer to float but okay to tie to V_{IH} or V_{IL}
B2	DC	NC	Do not connect	Internally pulled down. Prefer to float but okay to tie to V_{IH} or V_{IL}
B6	DC	NC	Do not connect	Prefer to float but okay to tie to V_{IH} or V_{IL}
E3	DC	V_{CAP}	Do not connect	**Must be kept at a Steady State.** Prefer floating or tied to V_{SS} to minimize current draw.
G2	NC	/HSB	No connect	Prefer to float but okay to tie to V_{IH} or V_{IL}

PACKAGE DIMENSIONS
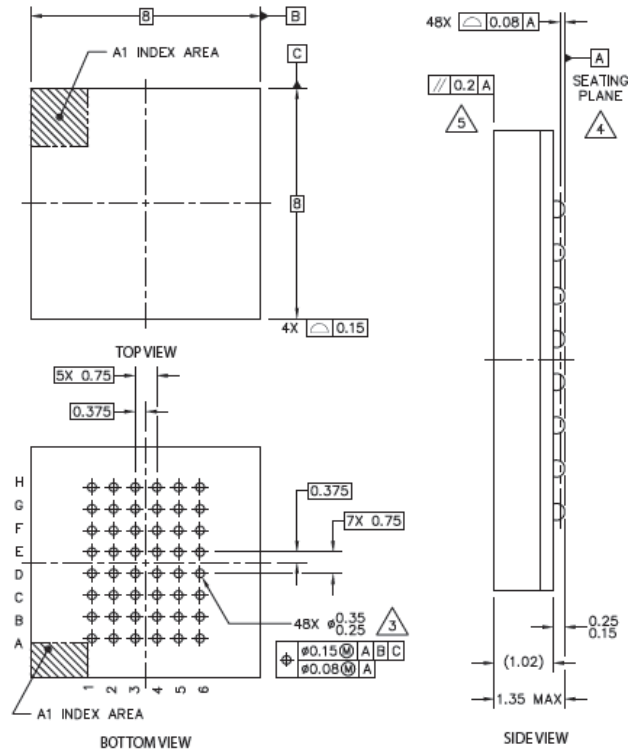
Figure 2 - Everspin BGA package dimensions
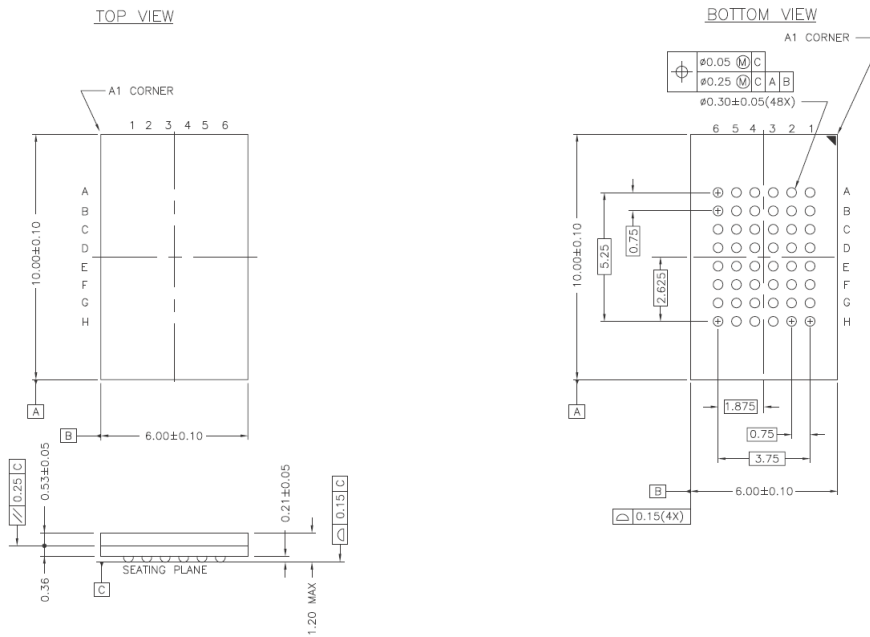
Figure 3 - Cypress BGA package dimensions

OTHER REPLACEMENT DESIGN CONSIDERATIONS

HSB SOFTWARE

Due to its persistence, there is no power monitoring requirement for the Everspin MRAM as is the case with the nvSRAM. Therefore, initiating or monitoring Hardware Stores, Re-stores and associated software routines are unnecessary and can be eliminated.

SIMPLIFIED POWER CYCLING

When power is removed from the MRAM, data remains indefinitely over time and temperature until re-programmed. This feature, unique to MRAM, allows for Duty Cycle Power control enabling the user to reduce their overall power consumption without the concern of wear-out.

MRAM requires control signals /E and /W to track the power supply during power-up and be held high for a 2ms start-up period a much shorter power-up requirement than the nvSRAM. When power fails, the Everspin MRAM simply inhibits write operations and no special power down timing considerations are needed since data is always non-volatile.

The nvSRAM device requires the /WE signal to track the power supply during power-up and be held high during the power-up recall period of 20ms. The nvSRAM must sense the power failure, decouple the power supply from its backup capacitor, wait for any SRAM operations to complete, and then perform a parallel write to the EEPROM storage element during the 8ms period after power has failed. This sequence is complicated by the fact that power falls at various ramp rates and in some cases bounces above and below the power supply threshold (brown outs) in rapid succession. Thus raising concerns about reliability of the backup storage cycle under all system power conditions including some that cannot easily be simulated or tested.

Additionally, there may be concern with the wear-out of nvSRAM EEPROM storage element which is limited to 1 million Program/Erase cycles. Everspin MRAM supports unlimited read, write, and power cycles. There are no wear-out concerns with MR256D08BMA45.

POWER-UP SEQUENCING

Both MRAM and nvSRAM will operate from a standard +3.3 volt power supply with +/-10% power supply range. Both MRAM and nvSRAM have similar standby and active operating currents, however, the "Start-up" time for the MRAM is 2ms vs. 20ms for the nvSRAM. Proper decoupling capacitors should be used to assure reliable operation.
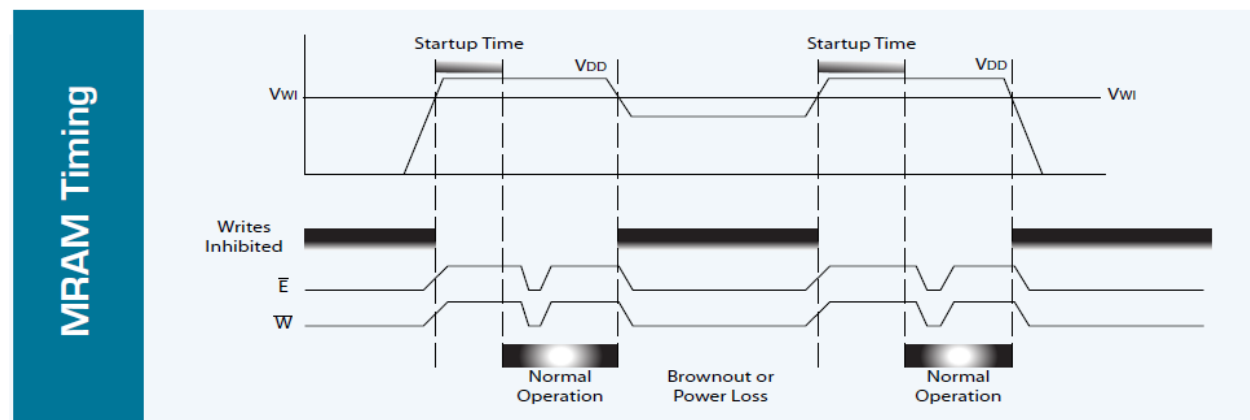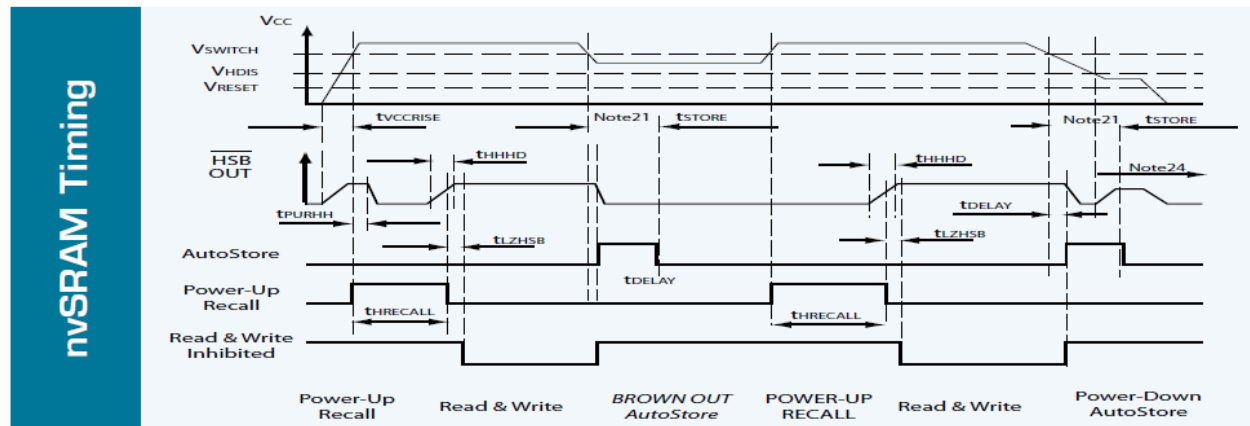
RELIABILITY CONSIDERATIONS FOR COMPARISON

CY14V256LA-BA35 uses conventional trapped charge technology for non-volatile storage. Data can leak away as wear-out results from temperature and excessive write cycles. Engineers must carefully design systems using nvSRAM to avoid exceeding the non-volatile write limitation of 1million cycles.

Everspin MRAM will provide the most cost effective non-volatile RAM solution. The nvSRAM is constructed by combining a standard 6-transistor SRAM with a non-volatile EEPROM storage element in every cell. The total cell complexity is 12-transistors. MR256D08BMA45 is built using a much simpler 1-transistor, 1-magnetic tunnel junction cell. The simple Everspin MRAM cell leads to improved manufacturing efficiency and increased reliability.

The reliability of an nvSRAM is dependent upon not only the memory chip but also the quality of the external V_{CAP} capacitor. Careful capacitor selection is necessary to assure reliable power sequencing.

MRAM uses magnetic tunnel junction technology for non-volatile storage. Data does not leak away at high temperature and there is no wear-out mechanism to limit the number of read, write, or power cycles. Data retention is better than 20 years at 125 °C.

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Replacing the Cypress CY14V256LA-BA35 nvSRAM with Everspin's MR256D08BMA45 MRAM
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