Using a Single V\textsubscript{DD} pin for the MR0D08BMA45

1Mb [128Kb x 8 configuration] Everspin MRAM in 48-ball BGA Package

INTRODUCTION

This Application Note is provided as a reference document substantiating the use of a single V\textsubscript{DD} supply for the MR0D08B MRAM Family in 48-BGA packages.

MR0D08B BGA PACKAGE DESIGN

The MR0D08B MRAM die is designed with four V\textsubscript{DD} pads that are electrically connected with negligible impedance (0.2 Ohms) between each pad. The BGA substrate used in manufacturing the device directly connects pins A6 and C2. Wire Bonds are attached between the substrate and each of the four V\textsubscript{DD} pads on the die as shown in the cross sections in the figures that follow. This double bonded structure allows for redundancy as well as an even distribution of I\textsubscript{DD}. Such a structure, while optimal for redundancy and distribution of I\textsubscript{DD} is not a requirement for operation.

EFFECT OF USING A SINGLE VDD PIN

The Current Carrying Capacity of each of the Bond Wires is sufficient to support the maximum load of the die under worst case conditions without impacting the performance of the IC. Tests conducted by the Package subcontractor validate the minimal impact of using a single V\textsubscript{DD} on this device. Tests have also validated that any resistance imbalance due to using a single V\textsubscript{DD} pin have proven to have minimal impact on the current distribution of the bond wires. It should be noted, that any increase in resistance and inductance due to using a single V\textsubscript{DD} pin may cause a voltage drop seen by the device under worst case conditions to be in the range of several 10’s of mV. Summarizing, adequate margin in the design of this device supports the use of a single V\textsubscript{DD} supply pin for the MR0D08B product family under worst case conditions.

NOTE:

Both A6 and C2 balls are internally connected to each other on the BGA package substrate. If only one ball is connected to V\textsubscript{DD} on the PCB, both balls will be at V\textsubscript{DD} potential and the unused ball/landing pad on the PCB must be left unconnected to anything other than V\textsubscript{DD}.
PACKAGE SIMULATION with Balls A6 and C2 connected to $V_{DD}$

Cross Sections

Connectivity from solder balls to die

Electrical Simulation

Package Electrical Characteristics (Test frequency 1GHz)

<table>
<thead>
<tr>
<th>Net Branch</th>
<th>R (mΩ)</th>
<th>$L_s$ (nH)</th>
<th>$L_m$ (nH)</th>
</tr>
</thead>
<tbody>
<tr>
<td>From Pads 13 and 14 to balls A6 and C2</td>
<td>168.8</td>
<td>2.21</td>
<td>0.03</td>
</tr>
<tr>
<td>From Pads 41 and 42 to balls A6 and C2</td>
<td>159.8</td>
<td>2.51</td>
<td></td>
</tr>
</tbody>
</table>

R - DC Resistance  $L_s$ - Self Inductance  $L_m$ - Mutual Inductance
PACKAGE SIMULATION with Ball A6 only connected to V_{DD}

Cross Sections

Connectivity from solder balls to die

Electrical Simulation

Package Electrical Characteristics (Test frequency 1GHz)

<table>
<thead>
<tr>
<th>Net Branch</th>
<th>R (mΩ)</th>
<th>Ls (nH)</th>
<th>Lm (nH)</th>
</tr>
</thead>
<tbody>
<tr>
<td>From Pads 13 and 14 to ball A6 only</td>
<td>388.06</td>
<td>6.12</td>
<td></td>
</tr>
<tr>
<td>From Pads 41 and 42 to ball A6 only</td>
<td>193.76</td>
<td>3.09</td>
<td>1.65</td>
</tr>
</tbody>
</table>

R - DC Resistance   Ls - Self Inductance   Lm - Mutual Inductance
TEST RESULTS

Access Times at 90°C

Access Times (ns) @ 90C, 3.0V

Access Times (ns) @ 90C, 3.3V

Access Times (ns) @ 90C, 3.6V

Access Times at -15°C

\( T_{WHAX} -15°C \) (ns)

\( T_{AVQV} -15°C \) (ns)
CONCLUSION

Review of the package interconnects of the MR0D08B device along with electrical simulation and statistically acceptable sample results confirm the use of a single \( V_{DD} \) for the MR0D08B. Summarizing, adequate margin in the design of this device supports the use of a single \( V_{DD} \) supply pin for the MR0D08B product family under worst case conditions.

NOTES:

1. A note of caution reminds the designer that though the use of both the A6 and C2 pins are not required for proper operation, due to the internal connection of these pins, it is important that any unused \( V_{DD} \) pin remains isolated from use because \( V_{DD} \) will be present on the unused solder ball.
2. The designer is reminded to review the impact, if any, to their design due to the potential impedance change in the device as a result of using a single \( V_{DD} \).
Using a Single $V_{DD}$ pin for the
MR0D08BMA45

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Single Vdd for MR0D08B in 48-ball BGA Package_AppNote_EST1874_Rev1
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