Using a Single V_{DD} pin for the MR0D08BMA45

1Mb [128Kb x 8 configuration] Everspin MRAM in 48-ball BGA Package

INTRODUCTION

This Application Note is provided as a reference document substantiating the use of a single V_{DD} supply for the MR0D08B MRAM Family in 48-BGA packages.

> **NOTE:**
> Both A6 and C2 balls are internally connected to each other on the BGA package substrate. If only one ball is connected to V_{DD} on the PCB, both balls will be at V_{DD} potential and the unused ball/landing pad on the PCB must be left unconnected to anything other than V_{DD}.

MR0D08B BGA PACKAGE DESIGN

The MR0D08B MRAM die is designed with four V_{DD} pads that are electrically connected with negligible impedance (0.2 Ohms) between each pad. The BGA substrate used in manufacturing the device directly connects pins A6 and C2. Wire Bonds are attached between the substrate and each of the four V_{DD} pads on the die as shown in the cross sections in the figures that follow. This double bonded structure allows for redundancy as well as an even distribution of I_{DD}. Such a structure, while optimal for redundancy and distribution of I_{DD} is not a requirement for operation.

EFFECT OF USING A SINGLE VDD PIN

The Current Carrying Capacity of each of the Bond Wires is sufficient to support the maximum load of the die under worst case conditions without impacting the performance of the IC. Tests conducted by the Package subcontractor validate the minimal impact of using a single V_{DD} on this device. Tests have also validated that any resistance imbalance due to using a single V_{DD} pin have proven to have minimal impact on the current distribution of the bond wires. It should be noted, that any increase in resistance and inductance due to using a single V_{DD} pin may cause a voltage drop seen by the device under worst case conditions to be in the range of several 10’s of mV. Summarizing, adequate margin in the design of this device supports the use of a single V_{DD} supply pin for the MR0D08B product family under worst case conditions.

PACKAGE SIMULATION with Balls A6 and C2 connected to V_{DD}

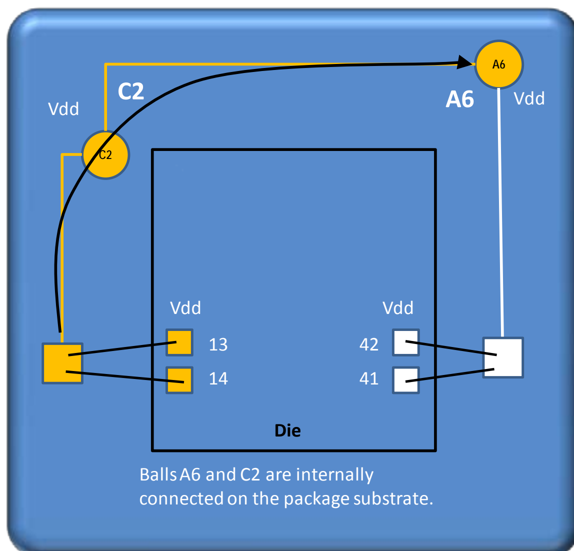
Cross Sections

Connectivity from solder balls to die

Electrical Simulation

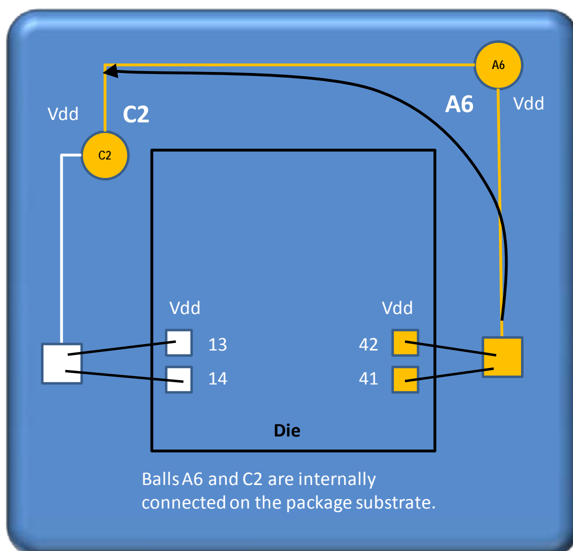
Package Electrical Characteristics (Test frequency 1GHz)

Top View – Not to Scale



Pads 13, 14 to balls C2 and A6

Top View – Not to Scale



Pads 41, 42 to balls A6 and C2

Net Branch	R (mΩ)	Ls (nH)	Lm (nH)
From Pads 13 and 14 to balls A6 and C2	168.8	2.21	0.03
From Pads 41 and 42 to balls A6 and C2	159.8	2.51	

R - DC Resistance   Ls - Self Inductance   Lm - Mutual Inductance

PACKAGE SIMULATION with Ball A6 only connected to V_{DD}

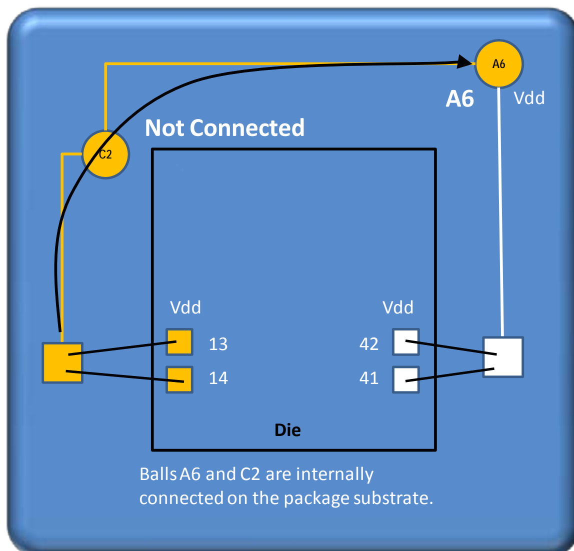
Cross Sections

Connectivity from solder balls to die

Electrical Simulation

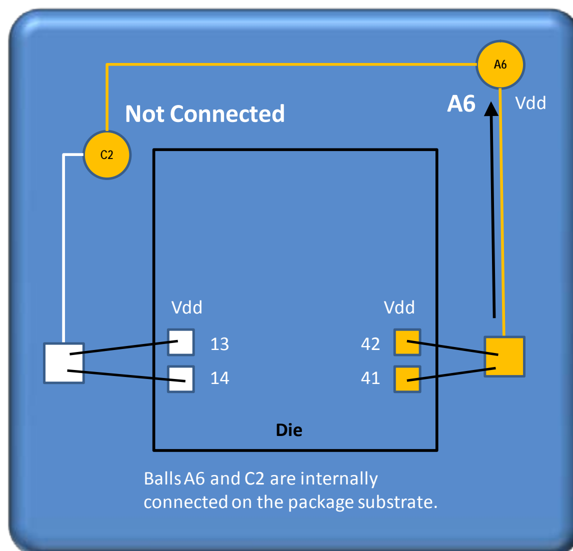
Package Electrical Characteristics (Test frequency 1GHz)

Top View – Not to Scale



Pads 13, 14 to balls C2 and A6

Top View – Not to Scale



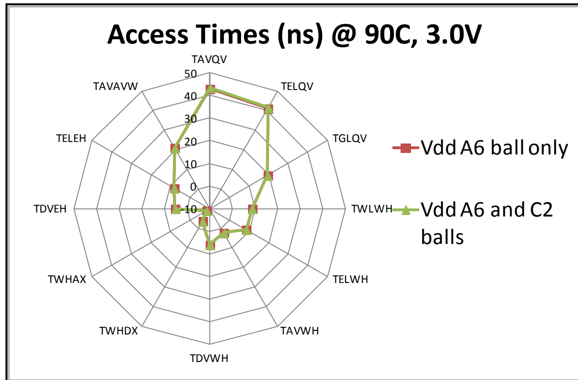
Pads 41, 42 to balls A6 and C2

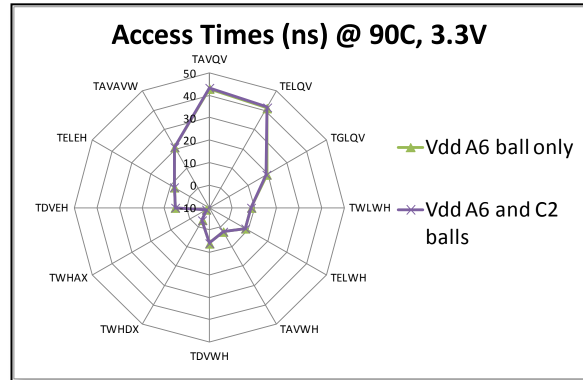
<table>
<tr><th>Net Branch</th><th>R (mΩ)</th><th>Ls (nH)</th><th>Lm (nH)</th></tr>
<tr><td>From Pads 13 and 14 to ball A6 only</td><td>388.06</td><td>6.12</td><td rowspan="2">1.65</td></tr>
<tr><td>From Pads 41 and 42 to ball A6 only</td><td>193.76</td><td>3.09</td></tr>
</table>

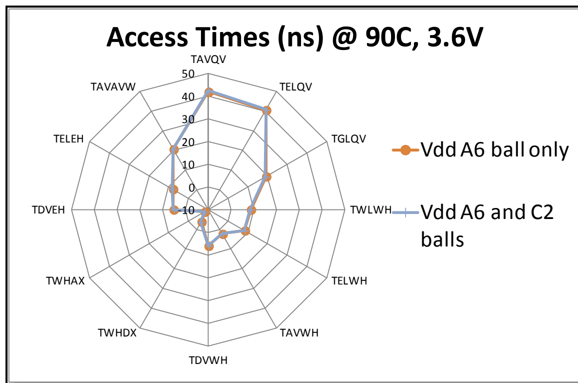
R - DC Resistance   Ls - Self Inductance   Lm - Mutual Inductance

TEST RESULTS

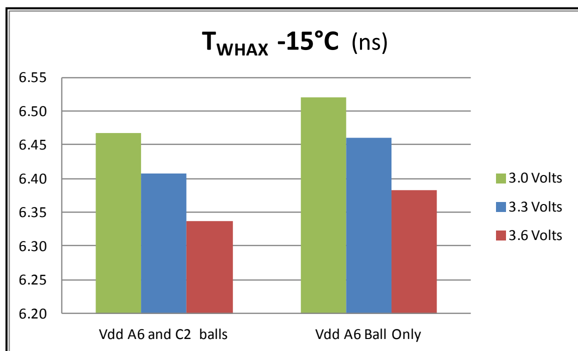
Access Times at 90°C

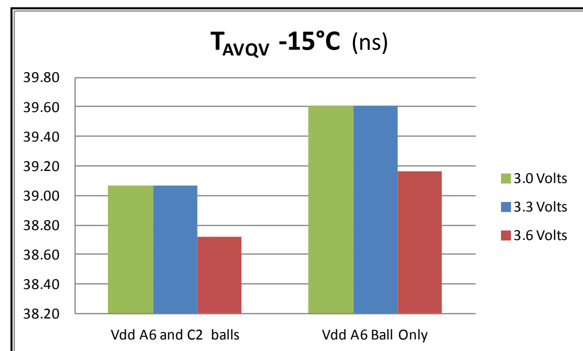






Access Times at -15°C





CONCLUSION

Review of the package interconnects of the MR0D08B device along with electrical simulation and statistically acceptable sample results confirm the use of a single V_{DD} for the MR0D08B. Summarizing, adequate margin in the design of this device supports the use of a single V_{DD} supply pin for the MR0D08B product family under worst case conditions.

NOTES:

1. A note of caution reminds the designer that though the use of both the A6 and C2 pins are not required for proper operation, due to the internal connection of these pins, it is important that any unused V_{DD} pin remains isolated from use because V_{DD} will be present on the unused solder ball.
2. The designer is reminded to review the impact, if any, to their design due to the potential impedance change in the device as a result of using a single V_{DD}.

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