Replacing the Cypress CY14B108LA-xx 8Mb nvSRAM with Everspin's MR4A08Bxxx 16Mb MRAM

GENERAL CONSIDERATIONS for REPLACING nvSRAM with MRAM

Every write with an MRAM is instantly non-volatile for at least 20 years. There is no transfer of data from a volatile to a non-volatile memory cell, no external capacitors or back up batteries. The elimination of external components, highly reliable data retention, and 35ns SRAM compatible READ/WRITE access times make the Everspin MR4A08xxx 16Mb MRAM a viable candidate for increasing system memory density by replacing the Cypress CY14B108LA-xx 8Mb nvSRAM without major PCB changes while reducing system cost without compromising system performance.

EVERSPIN MRAM MEMORY

Everspin is the global leader in commercially viable MRAM technology and Everspin MRAM products are present in hundreds of applications demanding high-speed, reliable, non-volatile memory.

MR4A08Bxxx COMPARISON TO CY14B108LA-xx

The Everspin MRAM solution provides:

- Immediate (<1ns) Power-off with no loss of data
- Always Non-Volatile. No Unreliable Capacitor Dependent Backup Cycles
- No Vcap or Vbatt required
- No complex Software STORE/RECALL routines
- 20-Year Data Retention with No Cycling Dependence
- Fewer components means smaller design footprint and lower total BOM cost
- No Wear-out Concerns
- Directly replaces the Cypress nvSRAM

COMPATIBILITY

The Everspin and MR4A08BxMA (48-BGA) memory is pin and timing compatible with the Cypress CY14B108LA-BA nvSRAM. The MR4A08BxYS and CY14B108LA-ZS are NOT drop in compatible. Please see PIN COMPATIBILITY for differences in pin out for the 44-TSOP2 package.

TIMING COMPATIBILITY

Both Everspin MRAM and nvSRAM have standard, compatible asynchronous SRAM timing. The MRAM however, retains data even at power off for an indefinite period of time and over temperature cycling. With a 35 ns read/write cycle time, the MRAM is compatible with similar nvSRAM speed grade options.

It is important to note that the Everspin MR4A08Bxxx device requires a minimum of 12ns hold time from Write Enable (and Chip Enable) high to Address invalid (Please see T_{WHAX} and T_{EHAX} in the MR4A08B data sheet available here.) Most microprocessors can accommodate this Hold time.

PIN COMPATIBILITY

- 16Mb organized in the 2Mbx8 configuration
- 3.3 volt nominal operation
- Standard SRAM parallel address pins (A0-19 (20 for 16Mb))
- Standard byte-wide, bidirectional data pins (DQ0-7)
- Standard control signals (/E, /W, /G)

The MR4A08B does not require an external capacitor and the other associated passive components required by the CY14B108LA-xx devices.

The primary differences between the Cypress and Everspin devices are the following:

The two pins on the nvSRAM: VCAP and /HSB (these pins are used to support the nvSRAM backup cycle and are not required for operation of the MRAM)

The Address lines for A19 and A20. Please see PIN COMPATIBILITY for the details.

V_{CAP} pin

A capacitor is required on the V_{CAP} pins (Pin 30 on the TSOP2 and Ball E3 on the BGA) on nvSRAM devices. Everspin assigns a "Do Not Connect" (DC) to these corresponding pins. It is preferred that these pins be left floating (Not Connected), however grounding these pins is acceptable.

/HSB pin

44-TSOP2

The /HSB pin of the TSOP2 package (pin 44 pin) should not be connected on the MRAM or always pulled low.

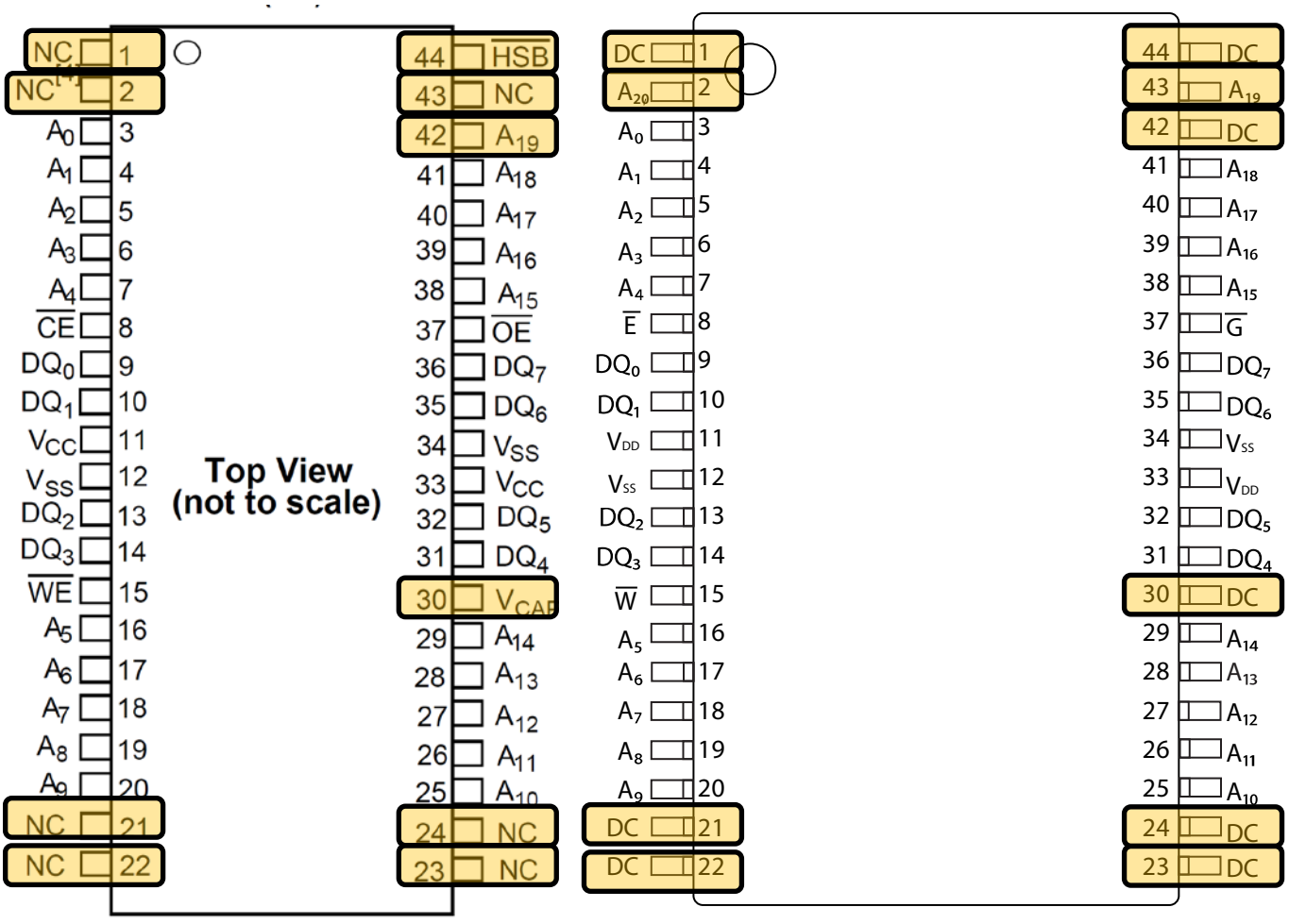
BGA

The /HSB ball on the BGA (G2) is corresponds to the A20 ball for the MRAM. This ball should be either pulled high or pulled low during Read and Write cycles.

Note that the ball on the MRAM corresponding to the /HSB ball on the nvSRAM will not assert the /HSB signal low (indicating a busy condition as is the case with the nvSRAM during a STORE cycle). Consequently, a Host processor should not expect the MRAM to assert the /HSB signal low.

PIN COMPATIBILITY

Figure 1 – Cypress 8Mb nvSRAM to Everspin 16Mb MRAM Pin Differences
44-TSOP2 Package



PIN COMPATIBILITY

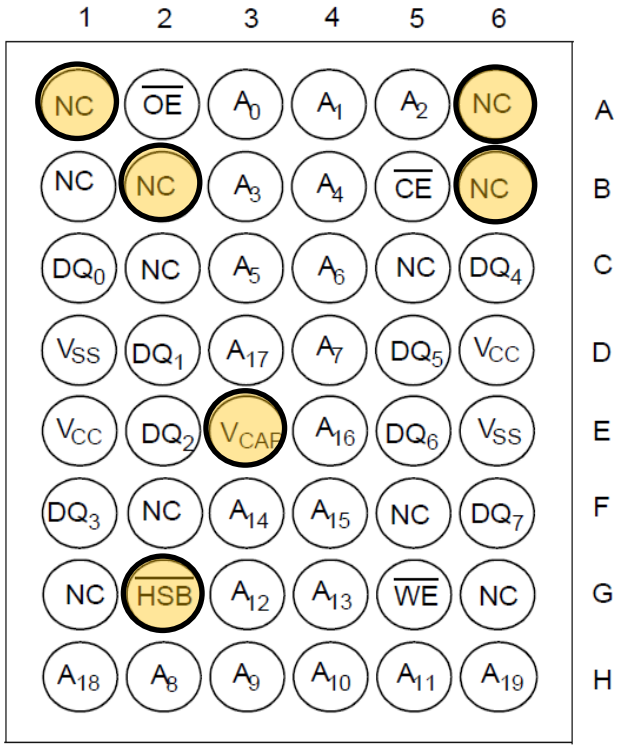
Table 1 - Cypress 8Mb nvSRAM to Everspin 16Mb MRAM Pin Differences
44 -TSOP2 Package

PIN #	Everspin	Cypress	Everspin Connection	Everspin Comments
1	DC	NC	Do Not Connect	Do Not Connect -Prefer to float or pulled low
2	A20	NC	A20 for 16Mb	A20
21	DC	NC	Do Not Connect	Do Not Connect -Prefer to float or pulled low
22	DC	NC	Do Not Connect	Do Not Connect -Prefer to float or pulled low
23	DC	NC	Do Not Connect	Do Not Connect -Prefer to float or pulled low
24	DC	NC	Do Not Connect	Do Not Connect -Prefer to float or pulled low
30	DC	VCAP	Do Not Connect	Do Not Connect -Prefer to float or pulled low
42	DC	A19	Do Not Connect	Do Not Connect -Prefer to float or pulled low
43	A19	NC	A19	A19
44	DC	/HSB	Do Not Connect	Do Not Connect -Prefer to float or pulled low

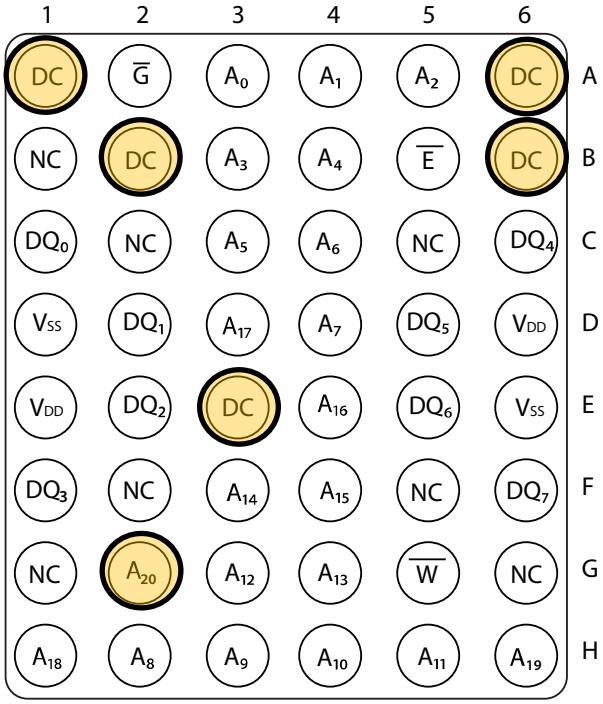
PIN COMPATIBILITY

Figure 2 – Cypress 8Mb nvSRAM to Everspin 16Mb MRAM Pin Differences
48-FBGA Package

CYPRESS



EVERSPIN



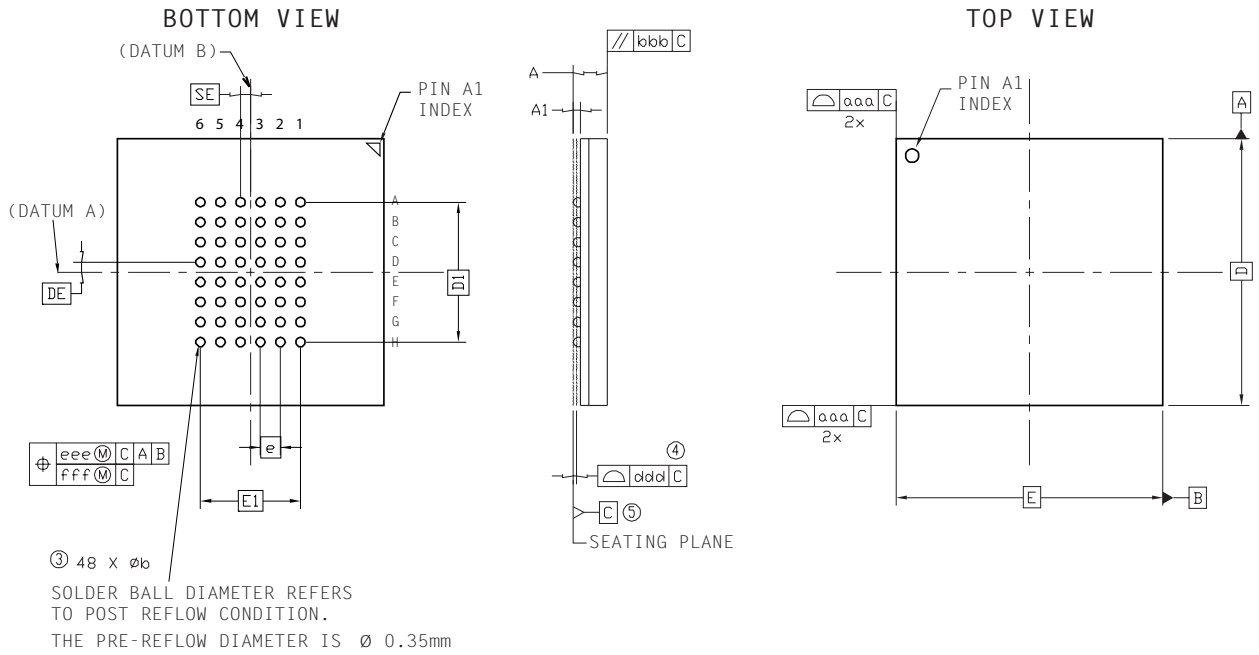
PIN COMPATIBILITY

Table 2 – Cypress 8Mb nvSRAM to Everspin 16Mb MRAM Pin Differences 48-FBGA Package

PIN #	Everspin	Cypress	Everspin Connection	Everspin Comments
A1	DC	NC	Do Not Connect	Do Not Connect -Prefer to float or pulled low
A6	DC	NC	Do Not Connect	Do Not Connect -Prefer to float or pulled low
B2	DC	NC	Do Not Connect	Do Not Connect -Prefer to float or pulled low
B6	DC	NC	Do Not Connect	Do Not Connect -Prefer to float or pulled low
E3	DC	Vcap	Do Not Connect	Do Not Connect -Prefer to float or pulled low
G2	A20	/HSB	A20 for 16Mb	Pull either high or low

PACKAGE COMPARISON

Figure 3 –Everspin 16Mb x8 MRAM 48-FBGA Package



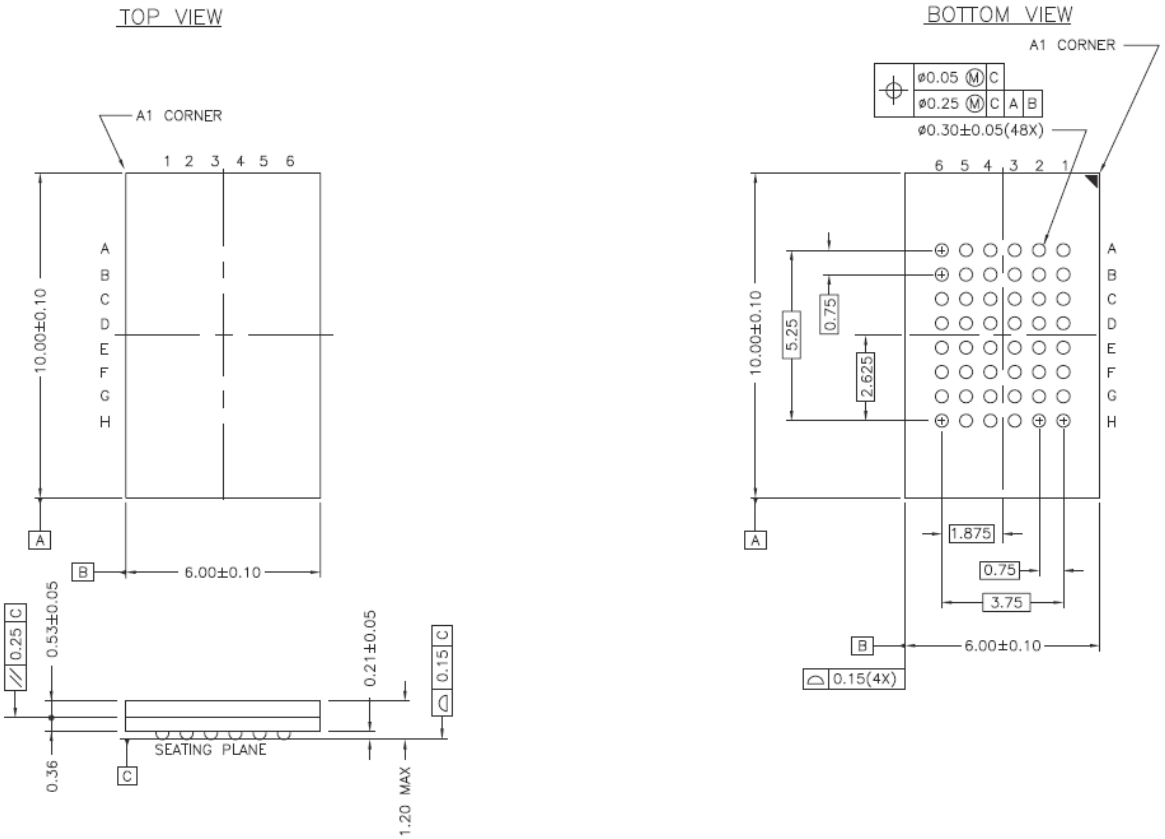
Ref	Min	Nominal	Max
A	1.19	1.27	1.35
A1	0.22	0.27	0.32
B	0.31	0.36	0.41
D	10.00 BSC		
E	10.00 BSC		
D1	5.25 BSC		
E1	3.75 BSC		
DE	0.375 BSC		
SE	0.375 BSC		
e	0.75 BSC		
Ref	**Tolerance of, from and position**		
aaa	0.10		
Bbb	0.10		
Ddd	0.12		
eee	0.15		
fff	0.08		

Print Version Not To Scale

1. Dimensions in Millimeters.
2. The 'e' represents the basic solder ball grid pitch.
3. 'b' is measurable at the maximum solder ball diameter in a plane parallel to datum C.
4. Dimension 'ccc' is measured parallel to primary datum C.
5. Primary datum C (seating plane) is defined by the crowns of the solder balls.
6. Package dimensions refer to JEDEC MO-205 Rev. G.

PACKAGE COMPARISON

Figure 4 –Cypress 8Mb x8 MRAM 48-FBGA Package



OTHER REPLACEMENT DESIGN CONSIDERATIONS

HSB SOFTWARE

Due to its persistence, there is no power monitoring requirement for the Everspin MRAM as is the case with the nvSRAM. Hence initiating or monitoring Hardware Stores, Re-stores and associated software routines are unnecessary and can be eliminated.

SIMPLIFIED POWER CYCLING

When power is removed from the MRAM, data remains valid over 20 years time and across the temperature range This feature, unique to MRAM, allows for Duty Cycle Power control enabling the user to reduce their overall power consumption without the concern of wear-out or loss of data.

MRAM requires control signals /E and /W to track the power supply during power-up and be held high for a 2 ms start-up period a much shorter power-up requirement than the

nvSRAM. When power fails, the Everspin MRAM simply inhibits write operations and no special power down timing considerations are needed since data is always non-volatile.

The nvSRAM device requires the /WE signal to track the power supply during power-up and be held high during the power-up recall period of 20 ms. The nvSRAM must sense the power failure, decouple the power supply from its backup capacitor, wait for any SRAM operations to complete, and then perform a parallel write to the EEPROM storage element during the 8 ms period after power has failed. This sequence is complicated by the fact that power falls at various ramp rates and in some cases bounces above and below the power supply threshold (brown outs) in rapid succession. Such conditions are not easily simulated or tested raising concerns about the reliability of the backup storage cycle and the data in the EPROM.

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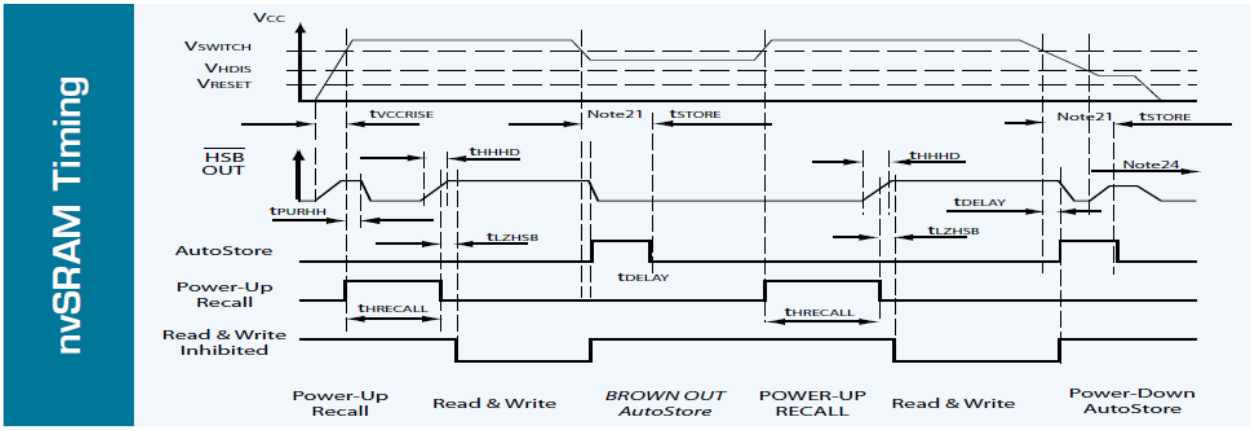
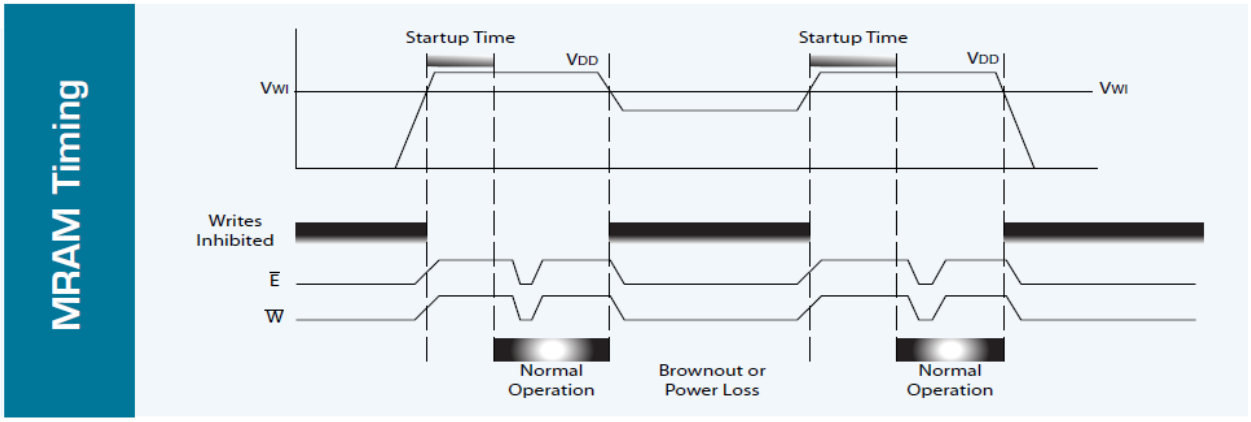
POWER-UP SEQUENCING

Both MRAM and nvSRAM will operate from a standard +3.3 volt power supply with +/-10% power supply range. Both MRAM and nvSRAM have similar standby and active operating currents, however the "Start-up" time for the MRAM is 2ms vs. 20ms for the nvSRAM. Proper decoupling capacitors should be used to assure reliable operation.





RELIABILITY CONSIDERATIONS FOR COMPARISON

CY14B108LA-xx uses conventional trapped charge technology for non-volatile storage. Data can leak away as wear-out results from temperature and excessive write cycles. Engineers must carefully design systems using nvSRAM to avoid exceeding the non-volatile write limitation of 1M cycles.

Everspin MRAM will provide the most cost effective non-volatile RAM solution. The nvSRAM is constructed by combining a standard 6-transistor SRAM with a non-volatile EEPROM storage element in every cell. The total cell complexity is 12-transistors. MR4A08Bxxx is built using a much simpler 1-transistor, 1-magnetic tunnel junction cell. The simple Everspin MRAM cell leads to improved manufacturing efficiency and increased reliability.

The reliability of an nvSRAM is dependent upon not only the memory chip but also the quality of the external VCAP capacitor. Careful capacitor selection is necessary to assure reliable power sequencing.

MRAM uses magnetic tunnel junction technology for non-volatile storage. Data does not leak away at high temperature and there is no wear-out mechanism to limit the number of read, write, or power cycles in this technology. Data retention is better than 20 years at 125 °C.

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