

### MRAM TECHNOLOGY

MRAM or Magnetic Random Access Memory uses a 1 transistor – 1 magnetic tunnel junction (1T-1MTJ) architecture with the magnetic “state” of a ferromagnetic material as the data storage element. Because MRAM uses a magnetic state for storage (rather than charge which can “leak away” with time), MRAM offers significantly long Data Retention (+20 years) and unlimited endurance. Switching the magnetic polarization (Write Cycle) is the result of pulsing current in conductive lines above and below a Magnetic Tunnel Junction (MTJ) (see figure 1). The associated H-field from the current pulses changes the polarization of the Free Layer of a ferromagnetic material. Such magnetic switching requires no displacement of atoms or electrons which means there is no wear-out mechanism associated with MRAM. The Magnetic moment of the Free Layer relative to the Fixed Layer changes the impedance of the MTJ (see figure 2). This change in impedance represents the state of the data (“1” or “0”). Sensing (Read Cycle) is accomplished by measuring the impedance of the MTJ (figure 3). Read cycles in MRAM devices are non-destructive and relatively fast (35ns). Read operations are accomplished with a very low voltage across the MTJ, supporting unlimited operation over the part lifetime.

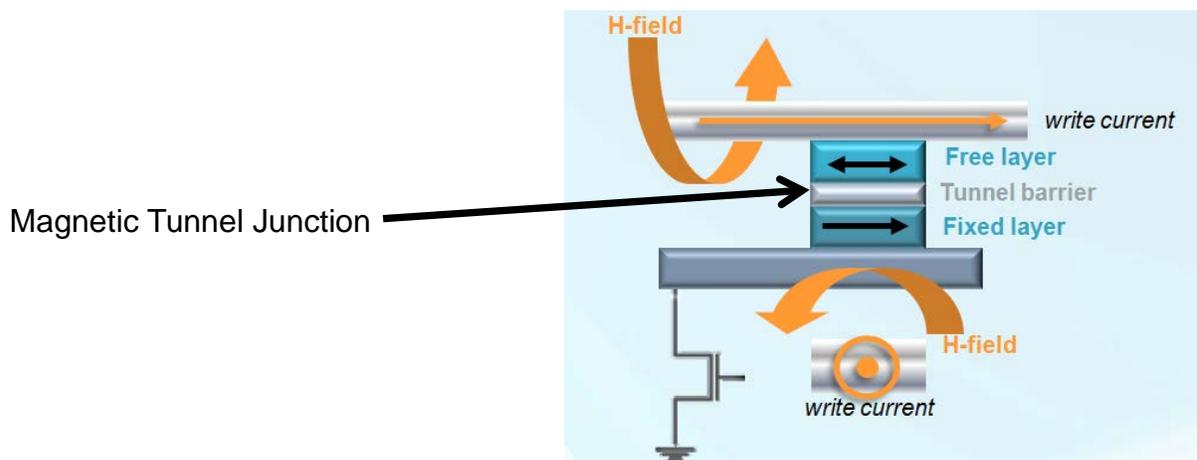


Figure 1: Magnetic Tunnel Junction (MTJ)

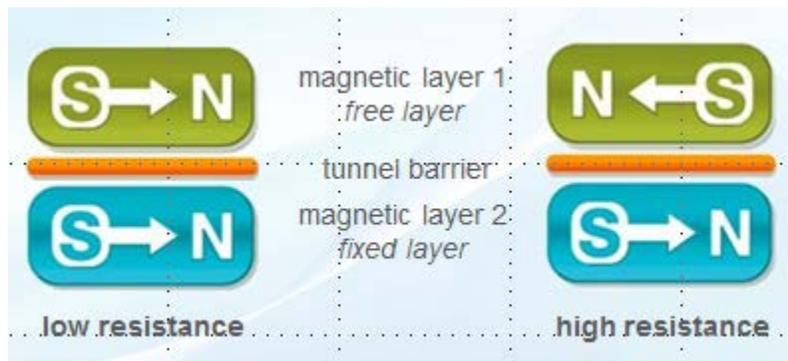


Figure 2: MRAM Magnetic Tunnel Junction (MTJ) Storage Element

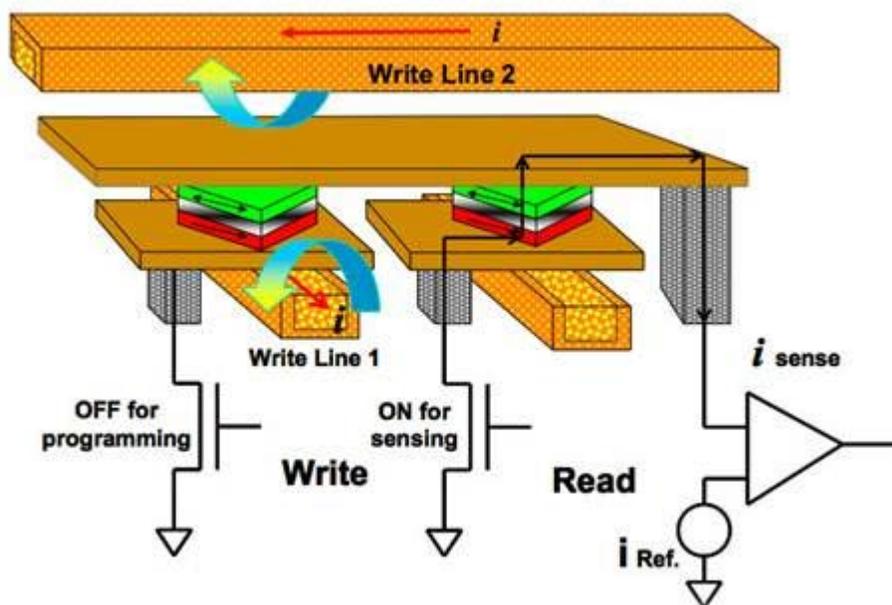


Figure 3: MRAM Write/Read cycle

### FRAM TECHNOLOGY

FRAM or Ferroelectric Random Access Memory uses a 1 transistor – 1 ferroelectric capacitor (1T-1FC) architecture that employs ferroelectric materials as storage devices. These materials have an intrinsic electric dipole switched into opposite polarities with an external electric field. Switching the ferroelectric polarization states requires the movement of the dipole ( $Ti^{4+}$  ion

located within an oxygen octahedron (in the case of  $\text{Pb}(\text{Zr,Ti})\text{O}_3$ ) in response to an electric field (figure 4). This movement can be impeded by a free electric charge or other ionic defects built-up over time and temperature. Such defects cause the dipoles to relax over time leading to fatigue.

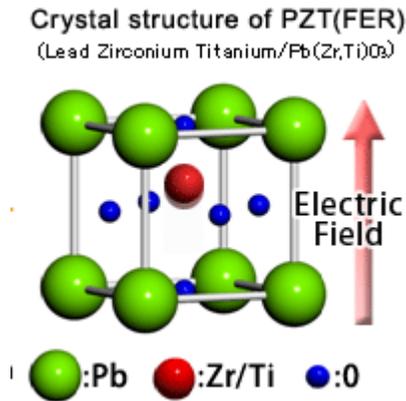


Figure 3: FRAM Atomic Structure

### Hysteresis Loop of PZT

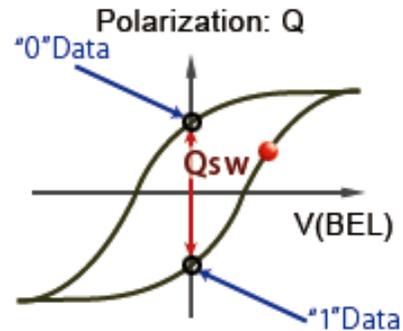


Figure 4: FRAM Data States

A read operation in a FRAM is destructive because it requires switching the polarization state in order to sense its state. The read operation has to restore the polarization to its original state after the initial read which adds cycle time to the read operation.

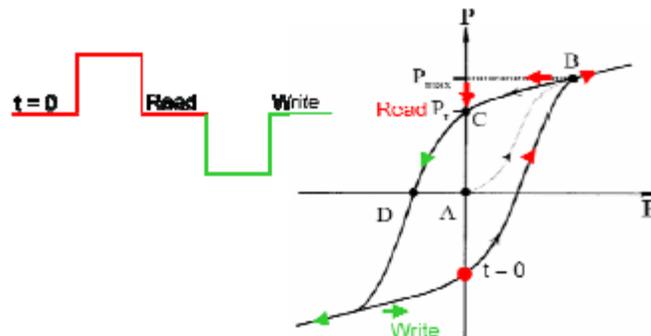


Figure 5: FRAM Write/Read cycle

FRAM Read and Write cycles require an initial “Pre-charge” time which can increase the initial access time.

### FATIGUE

As mentioned earlier, MRAM technology uses magnetic states for data storage. Switching the magnetic polarization between the two states does not require the motion of atoms and therefore, there is no wear-out mechanism for a MRAM device. Bit storage in an FRAM requires the movement of its inherent electric dipole ( $\text{Ti}^{4+}$  ion within the oxygen octahedron in the case of  $\text{Pb}(\text{Zr},\text{Ti})\text{O}_3$ ) in response to an electric field. Over time, dipole movement will be increasingly impeded by buildup of free electric charge in the capacitor and other ionic defects. Furthermore, hydrogen bonding with the ferroelectric dipole is a known wear-out mechanism, which is why  $\text{H}_2$  contamination is a concern in the CMOS BEOL manufacturing of FRAM.

### IMPRINT/OPPOSITE STATE RETENTION

FRAM technology has an inherent asymmetry in the hysteresis behavior of the memory elements. The bottom electrode has a higher thermal budget compared to the top electrode, causing a preferred dipole orientation of the ferroelectric element. Over time, this preferred orientation will eventually become so dominant that the external programming voltage will no longer be able to reorient the dipole out of the preferred orientation. The memory cell becomes locked into its preferred orientation causing a memory bit failure.

Another concern of FRAM technology is the reduction in polarization (signal) in response to lower read voltages. Full supply voltage is applied to the capacitor during write operations however, during read operations only part of the voltage is applied to the ferroelectric element because the Read voltage is divided between parasitic capacitance and ferroelectric capacitance. As a consequence, subsequent reads the voltage margin between states decreases and can eventually lead to an inability to differentiate between states.

### HIGH TEMPERATURE DATA RETENTION

Ambient operating temperatures above  $85^\circ\text{C}$  accelerate wear-out of FRAM due to build-up of free electric charge resulting in imprint.

Everspin MRAM has been demonstrated in carefully designed experiments to retain data for up to 20 years at  $125^\circ\text{C}$ .

### EXTENDED TEMPERATURE

Extended temperature FRAM (Industrial and Automotive (AEC-Q100 Grade 1)) typically requires the use of a 2T-2FC architecture. This architecture allows for a self-reference read compensating for a weakening polarization (signal margin) at higher operating temperatures.

Everspin MRAM requires no additional architecture changes to meet Industrial and Automotive temperature demands.

### MANUFACTURING

Everspin MRAM products are fabricated using standard commercial CMOS fabrication technology. The magnetic elements are built between two Cu metal layers, typically the last and next-to-last metal layers. There is no deviation from standard BEOL CMOS processing except for the addition of magnetic cladding layers in the metal trenches.

FRAM products are integrated on the W plug before the first BEOL metal layer. At the High temperatures of the FRAM process (650C required to deposit the PZT films) the W-plug is prone to oxidation making defect control a challenge.

Before returning to standard BEOL CMOS processing, the ferroelectric capacitors must be encapsulated in AlO<sub>x</sub> to prevent diffusion of H<sub>2</sub> into the other ferroelectric elements.

### SCALABILITY

At fabrication nodes of 65nm or smaller, 3D architecture will be required to build the ferroelectric (FRAM) elements. As the feature size decreases, the risk of Imprint, or non-preferred orientation of ferroelectric dipoles increases.

Everspin MRAM uses standard CMOS technology and has greater scalability with decreasing feature size without a significant cost premium.

### Comparing FRAM and MRAM (MR0A08A vs. FM28V100, 2.7V to 3.6V)

Attribute	FRAM	MRAM
<b>Technology</b>	1 transistor – 1 ferroelectric capacitor (1T – 1FRC)	1 transistor – 1 magnetic tunnel junction (1T – MTJ)
<b>Read</b>	Destructive	Non-destructive
<b>Read Cycle Time</b>	90ns	35ns
<b>Read Access Time</b>	60ns	35 ns
<b>Write Cycle Time</b>	90ns	35ns
<b>Write (CE)</b>	60ns	35ns
<b>Fatigue</b>	Known wear-out mechanisms $10^{14}$ Read / Write	No wear-out. Infinite Read / Write
<b>Imprint</b>	Increases with temperature and decreasing operating voltage	No Imprint
<b>High Temperature Data Retention</b>	Degrades above 85°C	20 years at 125°C (continuous)
<b>Manufacturing</b>	Complex – O <sub>2</sub> ambient >650°C process, H <sub>2</sub> sensitivity.	Standard BEOL CMOS processing
<b>Scalability</b>	Need 3D structures at 65nm. Imprint becomes more of an issue.	Fully Scalable

**Table 1: Attribute Comparison MRAM and FRAM**

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**Comparing FRAM and MRAM**

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