Replacing the Cypress CY14B101LA-xx nvSRAM with Everspin's MR0A08Bxxx MRAM

GENERAL CONSIDERATIONS for REPLACING nvSRAM with MRAM

Every write with an Everspin MRAM is instantly non-volatile for at least 20 years. There is no transfer of data from a volatile to a non-volatile memory cell, no external capacitors or back up batteries. The elimination of external components, highly reliable data retention, and 35ns SRAM compatible READ/WRITE Access times make the Everspin MRAM a viable candidate for replacing the Cypress CY14B101LA-xx nvSRAM without compromising system performance.

EVERSPIN MRAM MEMORY

Everspin is the global leader in commercially viable MRAM technology and Everspin MRAM products are present in dozens of applications demanding high-speed, reliable, non-volatile memory.

MR0A08B COMPARISON TO CY14B101LA

The Everspin MRAM solution provides:

- Always Non-Volatile. No Unreliable Capacitor Dependent Backup Cycles
- No Vcap or Vbatt required
- Immediate (<1ns) Power-off with no loss of data
- No complex Software STORE/RECALL routines
- Fast Star-up time (2ms vs. 20ms)
- Unlimited Read and Write cycles - No Wear-out Concerns
- 20-Year Data Retention with No Cycling Dependence
- Fewer components means smaller design footprint and lower total BOM cost
- Directly replaces the Cypress nvSRAM

COMPATIBILITY

The Everspin MR0A08BCYS (44-TSOP2) is pin and timing compatible with the Cypress CY14B101LA-ZS.

TIMING COMPATIBILITY

Both Everspin MRAM and nvSRAM have standard, compatible asynchronous SRAM timing. The MRAM however, retains data even at power off for an indefinite period of time and over temperature cycling. With a 35 ns read/write cycle time, the MRAM is compatible with similar nvSRAM speed grade options.

It is important to note that the Everspin MR0A08Bxxx device requires a minimum of 12ns hold time from Write Enable (and Chip Enable) high to Address invalid (Please see T_{WHAX} and T_{EHAX} in the MR0A08B data sheet available here.) Most microprocessors can accommodate this Hold time.

PIN COMPATIBILITY

- 1Mb organized in the 128Kx8 configuration
- 3.3 volt nominal operation
- Standard SRAM parallel address pins (A0-16)
- Standard byte-wide, bidirectional data pins (DQ0-7)
- Standard control signals (/E, /W, /G)

The MR0A08B does not require an external capacitor and the other associated passive components required by the CY14B101LA-xx devices.

The differences between the Cypress and Everspin devices are the two pins on the nvSRAM: V_{CAP} and /HSB. These pins are used to support the nvSRAM backup cycle and are not required for operation of the MRAM.

V_{CAP} pin

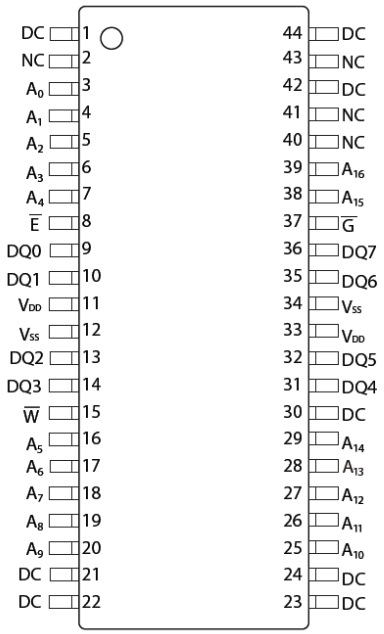
A capacitor is required on the V_{CAP} pins (Pin 30 on the TSOP2, Ball E3 on the BGA) on nvSRAM devices. Everspin assigns a "Do not connect" (DC) to the corresponding pins on the MRAM. When replacing the Cypress nvSRAM with the Everspin MRAM, it is recommended that this pin be either left floating or kept at V_{ss}. If a capacitor or V_{DD} is connected to this pin, it will have no effect on MRAM operation. However, the device may draw more current than if this pin is pulled to V_{ss} or left floating.

/HSB pin

The /HSB pin of the nvSRAM (Pin 44 of the TSOP2, Ball G2 on the BGA) is used to either initiate a Hardware Store or indicate a Hardware Store is in process. The pin 44 on the MRAM TSOP2 is recommended "Do not connect".

In the case of pin 44 on the TSOP2 package, the MRAM has a static pull-down to V_{ss}. Consequently, a Host processor should not expect the MRAM to drive this pin to a high state.

Everspin



Cypress

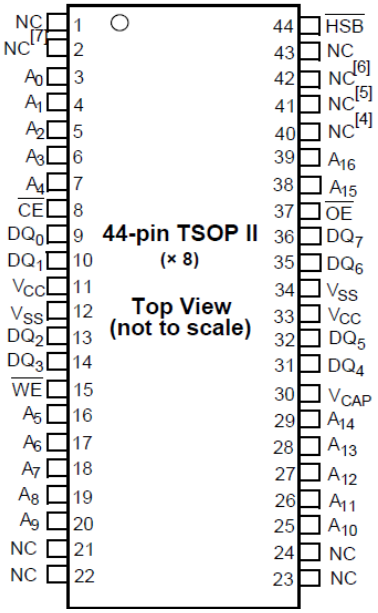


Figure 1 - Pin Function Comparison between MRAM and nvSRAM, 44 pin TSOP2 Package

PIN #	Everspin	Cypress	Everspin connection	Everspin Comments
1	DC	NC	Do not connect	Internally pulled down – okay to tie to VIH or VIL
2	NC	NC	Not connected to die	
21	DC	NC	Do not connect	Internally pulled down – okay to tie to VIH or VIL
22	DC	NC	Do not connect	Internally pulled down – okay to tie to VIH or VIL
23	DC	NC	Do not connect	Internally pulled down – okay to tie to VIH or VIL
24	DC	NC	Do not connect	Internally pulled down – okay to tie to VIH or VIL
30	DC	VCap	Do not connect	**Must be kept at a Steady State.** Prefer floating or tied to Vss to minimize current draw.
40	NC	NC	Not connected to die	
41	NC	NC	Not connected to die	
42	DC	NC	Do not connect	Internally pulled down – okay to tie to VIH or VIL
43	NC	NC	Not connected to die	
44	DC	HSB_	Do not connect	Internally pulled down. Ignore a low on this pin

Everspin **Cypress**

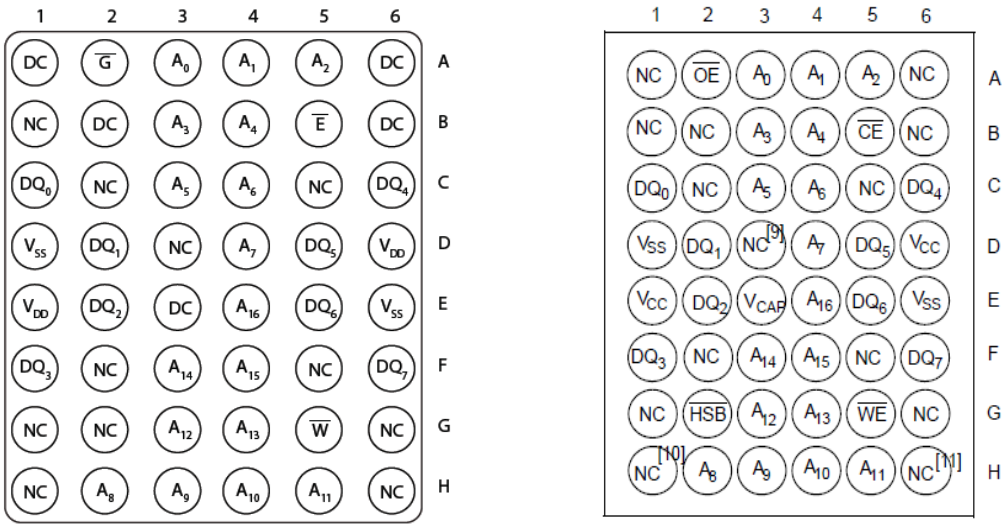


Figure 2 - Pin Function Comparison between MRAM and nvSRAM, 48 FBGA Package

PIN #	Everspin	Cypress	Everspin connection	Everspin Comments
A1	DC	NC	Do not connect	Internally pulled down. Prefer to float but okay to tie to VIH or VIL
A6	DC	NC	Do not connect	Prefer to float but okay to tie to VIH or VIL
B1	NC	NC	No connect	Prefer to float but okay to tie to VIH or VIL
B2	DC	NC	Do not connect	Internally pulled down. Prefer to float but okay to tie to VIH or VIL
B6	DC	NC	Do not connect	Prefer to float but okay to tie to VIH or VIL
C2	NC	NC	No connect	Prefer to float but okay to tie to VIH or VIL
C5	NC	NC	No connect	Prefer to float but okay to tie to VIH or VIL
D3	NC	NC	No connect	Prefer to float but okay to tie to VIH or VIL
E3	DC	VCap	Do not connect	**Must be kept at a Steady State.** Prefer floating or tied to Vss to minimize current draw.
F2	NC	NC	No connect	Prefer to float but okay to tie to VIH or VIL
F5	NC	NC	No connect	Prefer to float but okay to tie to VIH or VIL
G1	NC	NC	No connect	Prefer to float but okay to tie to VIH or VIL
G2	NC	HSB_	No connect	Prefer to float but okay to tie to VIH or VIL
G6	NC	NC	No connect	Prefer to float but okay to tie to VIH or VIL
H1	NC	NC	No connect	Prefer to float but okay to tie to VIH or VIL
H6	NC	NC	No connect	Prefer to float but okay to tie to VIH or VIL

Package Dimensions

The Everspin 44 pin TSOP2 device is drop in compatible with the corresponding Cypress equivalents. However, see Figures 3 and 4 to understand the package dimension differences between the Cypress and Everspin FBGA packages. Make special note of the package dimension differences requiring different mechanical "Keep out" areas for these packages.

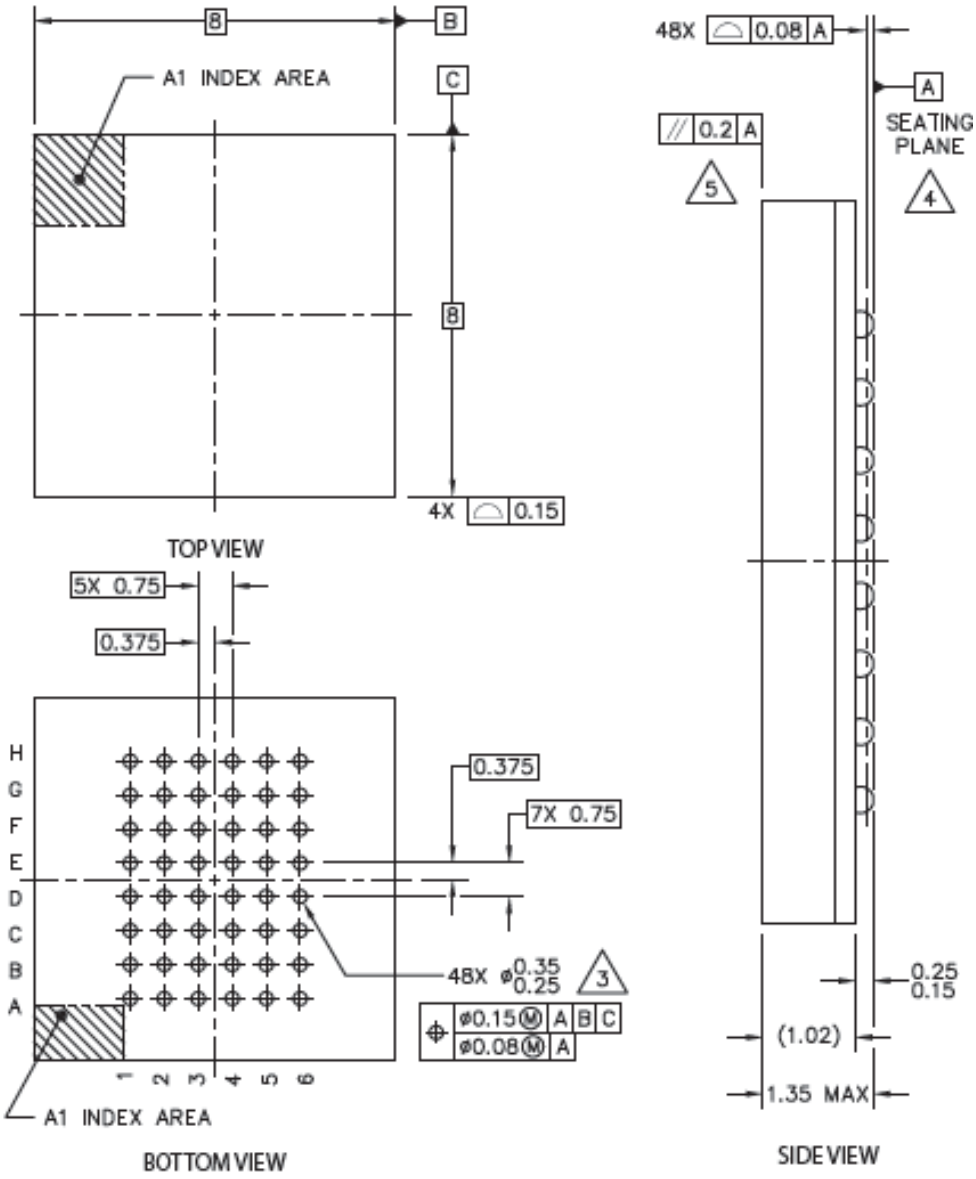


Figure 3 - Everspin FBGA Package Dimensions

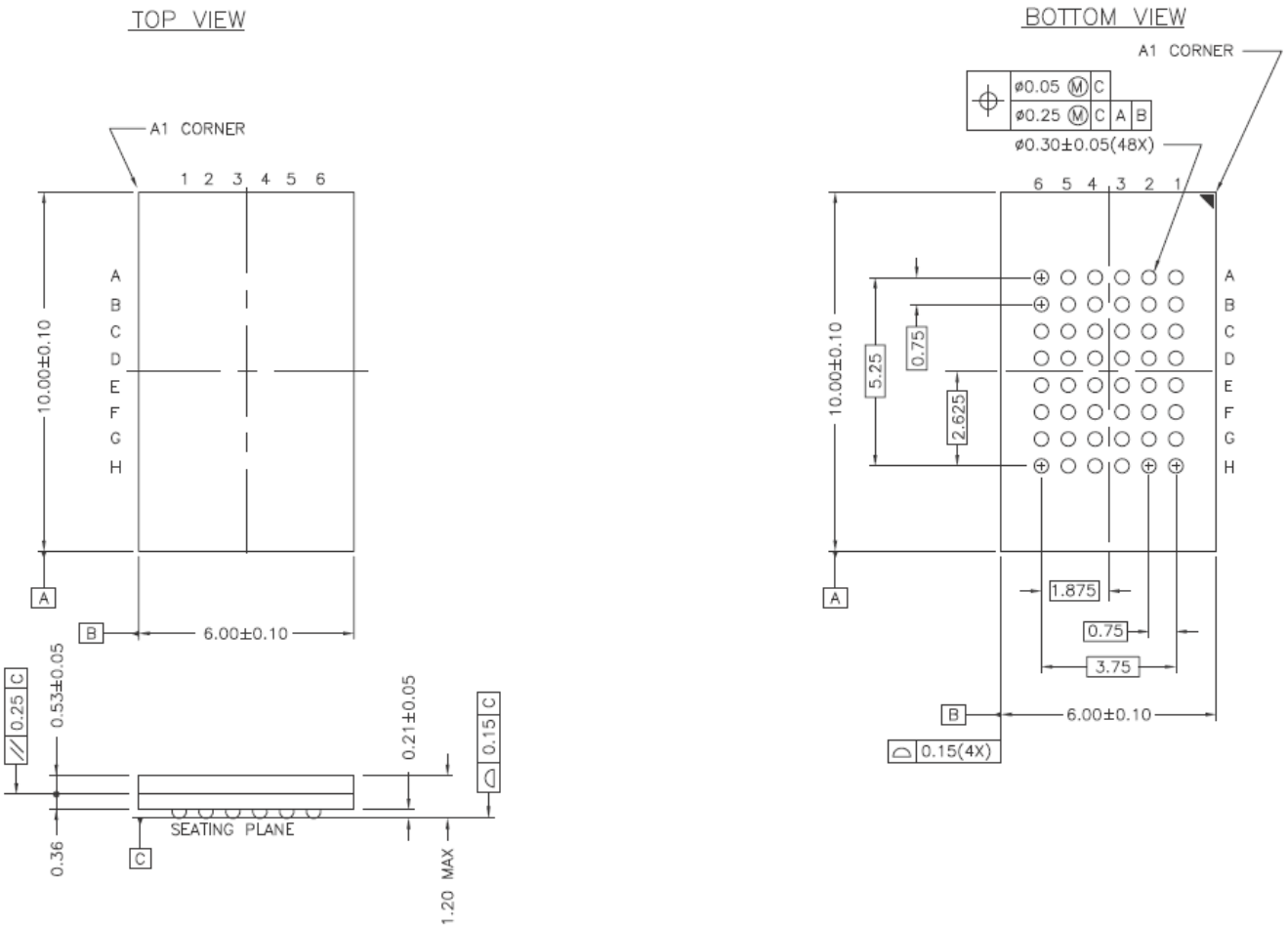


Figure 4 - Cypress FBGA Package Dimensions

OTHER REPLACEMENT DESIGN CONSIDERATIONS

HSB SOFTWARE

Due to its persistence, there is no power monitoring requirement for the Everspin MRAM as is the case with the nvSRAM. Therefore, initiating or monitoring Hardware Stores, Re-stores and associated software routines are unnecessary and can be eliminated.

SIMPLIFIED POWER CYCLING

When power is removed from the MRAM, data remains indefinitely over time and temperature until re-programmed. This feature, unique to MRAM, allows for Duty Cycle Power control enabling the user to reduce their overall power consumption without the concern of wear-out.

MRAM requires control signals /E and /W to track the power supply during power-up and be held high for a 2 ms start-up period a much shorter power-up requirement than the nvSRAM. When power fails, the Everspin MRAM simply inhibits write operations and no special power down timing considerations are needed since data is always non-volatile.

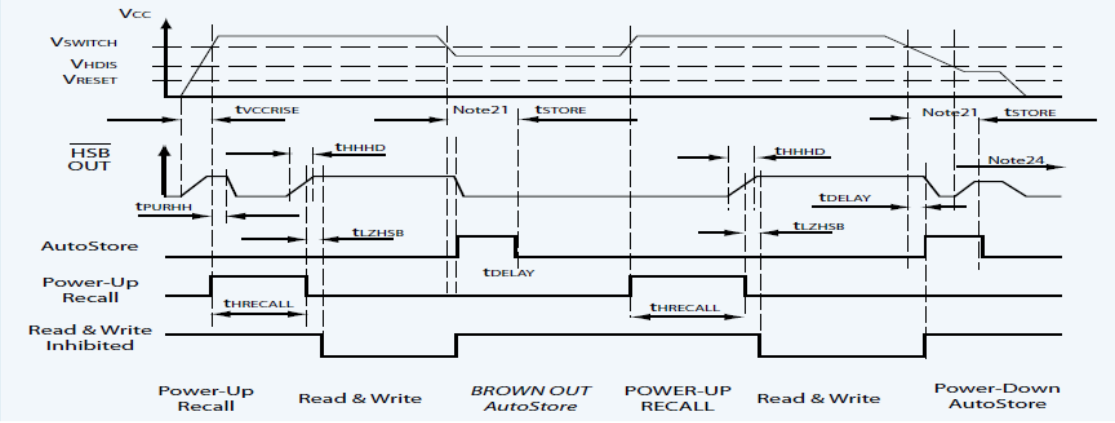
The nvSRAM device requires the /WE signal to track the power supply during power-up and be held high during the power-up recall period of 20 ms. The nvSRAM must sense the power failure, decouple the power supply from its backup capacitor, wait for any SRAM operations to complete, and then perform a parallel write to the EEPROM storage element during the 8 ms period after power has failed. This sequence is complicated by the fact that power falls at various ramp rates and in some cases bounces above and below the power supply threshold (brown outs) in rapid succession. Thus raising concerns about reliability of the backup storage cycle under all system power conditions including some that cannot easily be simulated or tested.

Additionally, there may be concern with wear-out of nvSRAM EEPROM storage element which is limited to just 200K cycles. Everspin MRAM supports unlimited read, write, and power cycles. There are no wear-out concerns with MR0A08Bxxx.

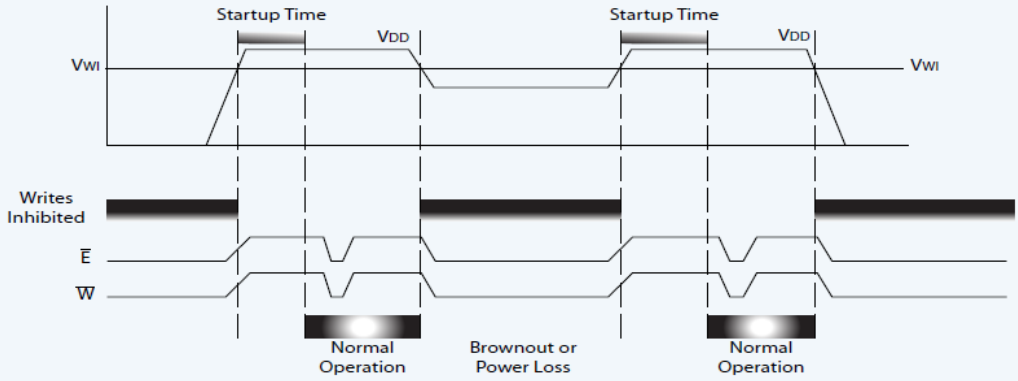
POWER-UP SEQUENCING

Both MRAM and nvSRAM will operate from a standard +3.3 volt power supply with +/-10% power supply range. Both MRAM and nvSRAM have similar standby and active operating currents, however, the "Start-up" time for the MRAM is 2ms vs. 20ms for the nvSRAM. Proper decoupling capacitors should be used to assure reliable operation.

nvSRAM Timing



MRAM Timing



RELIABILITY CONSIDERATIONS FOR COMPARISON

CY14B101LA-xx uses conventional trapped charge technology for non-volatile storage. Data can leak away as wear-out results from temperature and excessive write cycles. Engineers must carefully design systems using nvSRAM to avoid exceeding the non-volatile write limitation of 200K cycles.

Everspin MRAM will provide the most cost effective non-volatile RAM solution. The nvSRAM is constructed by combining a standard 6-transistor SRAM with a non-volatile EEPROM storage element in every cell. The total cell complexity is 12-transistors. MR0A08Bxxx is built using a much simpler 1-transistor, 1-magnetic tunnel junction cell. The simple Everspin MRAM cell leads to improved manufacturing efficiency and increased reliability.

The reliability of an nvSRAM is dependent upon not only the memory chip but also the quality of the external VCAP capacitor. Careful capacitor selection is necessary to assure reliable power sequencing.

MRAM uses magnetic tunnel junction technology for non-volatile storage. Data does not leak away at high temperature and there is no wear-out mechanism to limit the number of read, write, or power cycles in this technology. Data retention is better than 20 years at 125 °C.

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