

MR256A08B – 32K x 8 MRAM

VERILOG Model Readme File

Introduction

This is the VERILOG model for MR256A08B – a 32K x 8 MRAM Product from Everspin.

Device Summary

The **MR256A08B** is a 262,144-bit magnetoresistive random access memory (MRAM) device organized as 32,768 words of 16 bits. This device offers SRAM Compatible 35ns read/write operation and every data bit written into the memory is automatically protected in the MRAM array. Data retention of greater than 20 years is guaranteed. This device is offered in a 44 Pin TSOP II package and a 48 0.75mm Pitch BGA package.

Model Release Notes

Product Datasheet: http://www.everspin.com/PDF/EST_MR256A08B_prod.pdf

Model Revision: 1.0

Model Release Data: September 2010

Files

- | | |
|-----------------------|---------------------------------|
| 1. Readme_MR256A08B | - This File |
| 2. MR256A08B.v | - Device Model |
| 3. Config_MR256A08B.v | - File to Set Timing Parameters |

VERILOG Model

MR256A08B.v is the abstracted model of a 32K x 8 MRAM. The model is setup for a 35ns operation.

Warning: These VERILOG models are provided “as is” without warranty of any kind, including, but not limited to, any implied warranty of merchantability and fitness for a particular purpose.

Revision History

Date	Revision	Changes
9/26/2010	1.0	New Model – Initial Release

How to Reach Us:

Home Page:

www.everspin.com

E-Mail:

support@everspin.com

orders@everspin.com

sales@everspin.com

USA/Asia/Pacific

Everspin Technologies

1300 N. Alma School Road, CH-409

Chandler, Arizona 85224

+1-877-347-MRAM (6726)

+1-480-347-1111

Europe, Middle East and Africa

support.europe@everspin.com

Wokingham, United Kingdom

+44 (0)118 907 6155

Japan

support.japan@everspin.com

Yokohama, Japan

+81 (0) 45-846-6299

Document Number:

MR256A08B VERILOG Model, Revision 1, 9/2010

any integrated circuit or circuits based on the information in this document. Everspin Technologies reserves the right to make changes without further notice to any products herein. Everspin makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Everspin Technologies assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters, which may be provided in Everspin Technologies data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters including "Typicals" must be validated for each customer application by customer's technical experts. Everspin Technologies does not convey any license under its patent rights nor the rights of others. Everspin Technologies products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Everspin Technologies product could create a situation where personal injury or death may occur. Should Buyer purchase or use Everspin Technologies products for any such unintended or unauthorized application, Buyer shall indemnify and hold Everspin Technologies and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Everspin Technologies was negligent regarding the design or manufacture of the part. Everspin™ and the Everspin logo are trademarks of Everspin Technologies, Inc. All other product or service names are the property of their respective owners.

©

Information in this document is provided solely to enable system and software implementers to use Everspin Technologies products. There are no express or implied licenses granted hereunder to design or fabricate

