

MR0A16A – 64K x 16 MRAM

Verilog Model Readme File

Introduction

This is the VERILOG model for MR0A16A – a 64K x 16 MRAM Product from Everspin.

Device Summary

The **MR0A16A** is a 1,048,576-bit magnetoresistive random access memory (MRAM) device organized as 65,536 words of 16 bits. This device offers SRAM Compatible 35ns read/write operation and every data bit written into the memory is automatically protected in the MRAM array. Data retention of greater than 20 years is guaranteed. This device is offered in a 44 pin TSOP II package and a 48 ball 0.75mm Pitch BGA package

Model Release Notes

Product Datasheet: http://www.everspin.com/PDF/EST_MR0A16A_prod.pdf

Model Revision: 2.0

Model Release Data: February 2011

Model Files

- | | |
|---------------------|---------------------------------|
| 1. Readme_MR0A16A | - This File |
| 2. MR0A16A.v | - Device Model |
| 3. Config_MR0A16A.v | - File to Set Timing Parameters |

Test Bench

An example test bench which has been developed to verify this model is provided for user as a reference. The test bench checks the model against standard datasheet parameters and puts out error messages when certain parameters are violated.

Verilog Model

MR0A16A.v is the abstracted model of a 64K x 16 MRAM. The model is setup for a 35ns operation.

Warning: These Verilog models are provided “as is” without warranty of any kind, including, but not limited to, any implied warranty of merchantability and fitness for a particular purpose.

Revision History

Date	Revision	Changes
9/26/2010	1.0	New Model – Initial Release
2/10/2011	2.0	Updated model to cover corner cases and logic errors.

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