

# MR25H256 – 256Kb SPI MRAM

## VHDL Model Readme File

### Introduction

This is the VHDL model of the MR25H256 – a 256Kb SPI MRAM Product from Everspin. This is a high level abstraction of this product.

### Device Summary

The **MR25H256** is a 262,144-bit magnetoresistive random access memory (MRAM) device organized as 32,768 words of 8 bits. The **MR25H256** offers serial EEPROM and serial Flash compatible read/write timing with no write delays and unlimited read/write endurance. Unlike other serial memories, both reads and writes can occur randomly in memory with no delay between writes. The **MR25H256** is available in a small footprint 5 mm x 6 mm 8-pin DFN package that is compatible with serial EEPROM, Flash, and FeRAM products. Data Retention of greater than 20 years is guaranteed.

### Model Release Notes

Product Datasheet: [http://www.everspin.com/PDF/EST\\_MR25H256\\_prod.pdf](http://www.everspin.com/PDF/EST_MR25H256_prod.pdf)

Model Revision: 1.0

Model Release Data: August 2010

Model Test Tools: Mentor Graphics ModelSim, Symphony Sonata

### Files

- |                    |   |
|--------------------|---|
| 1. Readme_MR25H256 | - This File                                     |
| 2. MR25H256.vhdl   | - Device Model                                  |
| 3. Package_Utility | - Standard Conversion Utilities                 |
| 4. Benchtest.vhdl  | - Top Level Test Bench                          |
| 5. MR25H256.vhdl   | - Sample Test Vectors used for the Verification |
| 6. MR25H256.txt    | - Memory Initialization File                    |

### VHDL Model

MR25H256.vhdl is the abstracted model of the 256Kb SPI MRAM.

### Test Bench

Benchtest.vhdl and MR25H256\_driver.vhdl form the example test bench used to verify this model. This is not a complete test bench and has been provided to give information on model usage.

### Memory Initialization

MR25H256.txt is used to initialize the memory on startup. This file is updated on every memory write depending on the state of the MemoryUpdate Flag. The MemoryUpdate flag can be turned off to improve simulation speed or when data written into the MRAM array need not be saved.

The memory initialization file has the following format

```
FF FF FF FF .....FF
FF FF FF FF .....FF
```

Each row in the file has 1024 bytes of data. The MR25H256.txt has 32 rows.

**Warning:** These VHDL models are provided “as is” without warranty of any kind, including, but not limited to, any implied warranty of merchantability and fitness for a particular purpose.

## Revision History

Date	Revision	Changes
8/27/2010	1.0	New Model – Initial Release

### How to Reach Us:

Home Page:

[www.everspin.com](http://www.everspin.com)

### E-Mail:

[support@everspin.com](mailto:support@everspin.com)

[orders@everspin.com](mailto:orders@everspin.com)

[sales@everspin.com](mailto:sales@everspin.com)

### USA/Asia/Pacific

Everspin Technologies

1300 N. Alma School Road, CH-409

Chandler, Arizona 85224

+1-877-347-MRAM (6726)

+1-480-347-1111

### Europe, Middle East and Africa

[support.europe@everspin.com](mailto:support.europe@everspin.com)

Wokingham, United Kingdom

+44 (0)118 907 6155

### Japan

[support.japan@everspin.com](mailto:support.japan@everspin.com)

Yokohama, Japan

+81 (0) 45-846-6299

### Document Number:

**MR25H256, Revision 1, 8/2010**

Information in this document is provided solely to enable system and software implementers to use Everspin Technologies products. There are no express or implied licenses granted hereunder to design or fabricate any integrated circuit or circuits based on the information in this document. Everspin Technologies reserves the right to make changes without further notice to any products herein. Everspin makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Everspin Technologies assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters, which may be provided in Everspin Technologies data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters including "Typicals" must be validated for each customer application by customer's technical experts. Everspin Technologies does not convey any license under its patent rights nor the rights of others. Everspin Technologies products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Everspin Technologies product could create a situation where personal injury or death may occur. Should Buyer purchase or use Everspin Technologies products for any such unintended or unauthorized application, Buyer shall indemnify and hold Everspin Technologies and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Everspin Technologies was negligent regarding the design or manufacture of the part. Everspin™ and the Everspin logo are trademarks of Everspin Technologies, Inc. All other product or service names are the property of their respective owners.