

### Introduction

This is the VHDL model of the MR0A08B – a 128K x 8 MRAM Product from Everspin. This is a high level abstraction of this product.

### Device Summary

The **MR0A08B** is a 1,048,576-bit magnetoresistive random access memory (MRAM) device organized as 131,072 words of 8 bits. This device offers SRAM Compatible 35ns read/write operation and every data bit written into the memory is automatically protected in the MRAM array. Data retention of greater than 20 years is guaranteed. This device is offered in a 44 Pin TSOP II package and a 48 0.75mm Pitch BGA package.

### Model Release Notes

Product Datasheet: [http://www.everspin.com/PDF/EST\\_MR0A08B\\_prod.pdf](http://www.everspin.com/PDF/EST_MR0A08B_prod.pdf)

Model Revision: 1.0

Model Release Data: July 2010

Model Test Tools: Mentor Graphics ModelSim, Symphony Sonata

### Files

- |                        |   |
|------------------------|---|
| 1. Readme_MR0A08B      | - This File                                     |
| 2. MR0A08B.vhdl        | - Device Model                                  |
| 3. Package_Utility     | - Standard Conversion Utilities                 |
| 4. Benchtest.vhdl      | - Top Level Test Bench                          |
| 5. MR0A08B_Driver.vhdl | - Sample Test Vectors used for the Verification |
| 6. MR0A08B.txt         | - Memory Initialization File                    |

### VHDL Model

MR0A08B.vhdl is the abstracted model of the 128K x 8 MRAM. The model is setup for 35ns operation.

### Test Bench

Benchtest.vhdl and MR0A08B\_driver.vhdl form the example test bench used to verify this model. This is not a complete test bench and has been provided to give information on model usage.

### Memory Initialization

MR0A08B.txt is used to initialize the memory on startup. This file is updated on every memory write depending on the state of the MemoryWrite Flag. The MemoryWrite flag can be turned off to improve simulation speed or when data written into the MRAM array need not be saved.

The memory initialization file has the following format

```
FF FF FF FF .....FF
FF FF FF FF .....FF
```

Each row in the file has 1024 bytes of data. The MR4A08B.txt has 128 rows.

**Warning:** These VHDL models are provided “as is” without warranty of any kind, including, but not limited to, any implied warranty of merchantability and fitness for a particular purpose.

## Revision History

Date	Revision	Changes
7/30/2010	1.0	New Model – Initial Release

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