Introduction

This user guide is provided to help users understand the Hardware and Software requirements needed for evaluation of the EMxxLX Industrial STT MRAM device from Everspin.

This guide will outline the Hardware and Software requirements for the user to setup, configure, initialize, and generate traffic test vectors for the EMxxLX device.

This guide assumes the user has full access to the EMxxLX data sheet and a reasonable understanding of HW and SW usage. This guide makes references and links to other support documents for the user.

Contents

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List of Figures and Tables

1. EMxxLX Daughter Card

The EMxxLX Daughter Card is populated with Everspin EMxxLX 64Mbit Industrial STT MRAM device. Other EMxxLX densities can be populated as well. This device is obtained through the sample request form on Everspin's website located here:

https://www.everspin.com/xspi-industrial-iot-and-embedded-systems

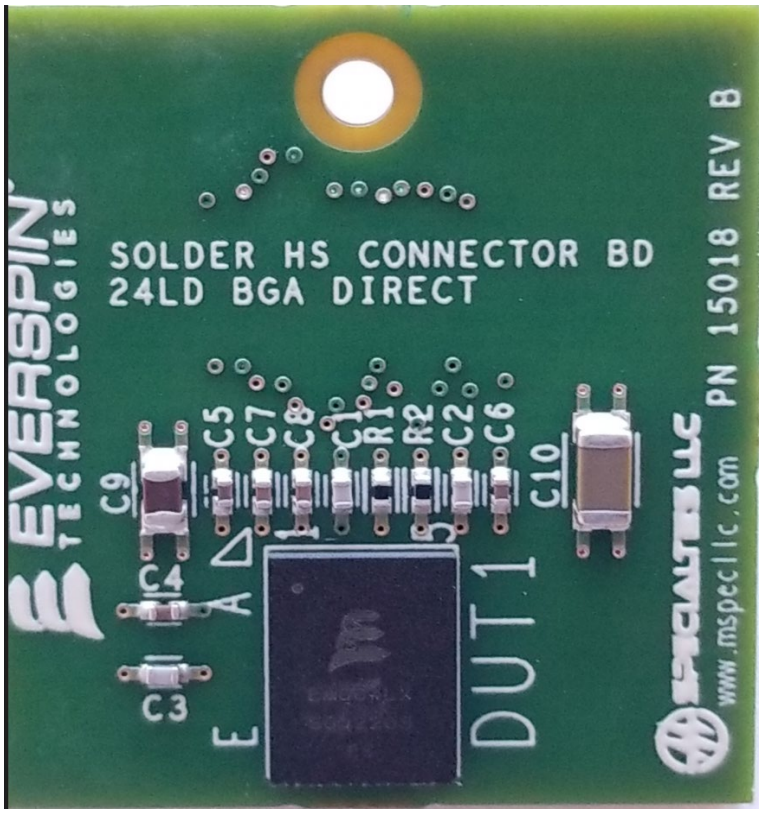

FIGURE 1 EMXXLX DAUGHTER CARD

2. Required Host Board Support

The EMxxLX evaluation board, here in referenced as the EMxxLX daughter card, is designed to connect to the Open FPGA specification Arrow AXE-5 Eagle host board HS (High Speed) slots. This host platform is available to order from Arrow Electronics Inc. website:

https://www.arrow.com/en/products/axe5-eagle-es/trenz-electronic-gmbh

The following features are available on the AXE-5 Eagle board:

System

FPGA Device

- Intel Agilex® 5 E-Series SoC FPGA device:
  - A5ED065BB32AE4SR0 (Engineering Silicon)
  - A5ED043BB32AE4S (Production FPGA)

Board Management System

- Power Monitor
- Temperature Monitor
- Fan Control
- Configurable Clock Source

FPGA Configuration and Debug

- 10-pin header for USB Blaster Programmer – JTAG mode
- 2 Gbit QSPI Flash – AS x4 Configuration scheme
- Partial reconfiguration support
- Support for Configuration via Protocol (CvP) through the PCI Express interface

FPGA Side

Memory Devices

- 8 Gbit 2133 MHz LPDDR4, 32 bits
- 2 Gbit QSPI Flash memory
- 2x 2 kbit serial MAC-Address EEPROMs
- 128 kbit EEPROM

Communication and Connectivity

- VITA 57.4 FMC+ Connector with 8 serial transceivers (8 RX and 8 TX)
- PCIe Gen4 x4 Edge connector
- 2x SFP+ connectors with up to 16 Gbps data rate
- 10/100/1000 Mbps Ethernet with TSN support via RJ45 connector
- HDMI 1.4 Transmitter with HDMI connector
- 2x CRUVI HS Connectors with MIPI D-PHY v2.5 interface
- 2x CRUVI LS Connectors
- 8-Channel, 12-Bit configurable ADC/DAC

HPS Side

Memory Devices

- 8 Gbit 2133 MHz LPDDR4, 32 bits

- microSD Card socket

Communication and Connectivity

- 10/100/1000 Mbps Ethernet with TSN support via RJ45 connector
- 4x USB-A 3.2 Gen1 Connectors
- USB to UART Bridge with Micro-USB Connector

Others

Buttons and Indicators

- 4x user RGB LEDs
- 2x green user LEDs
- 3x board status LEDs
- 7x push buttons
- 3x 4POS DIP switches

Power

- 2x 3 PCIe auxiliary power input connector for PCIe add-in operation
- DC Jack power input connector for standalone operation
- Recommended external supply voltage range: +12.0 V, 6.25 A (nominal)
- Recommended I/O signal voltage ranges:

o FMC+ interface: 0 to +1.3 V1
o CRUVI HS interface: 0 to +1.3 V1
o CRUVI LS interface: 0 to +3.3 V
o ADC analog input: 0 to +2.5 V
o ADC digital input: 0 to +3.3 V

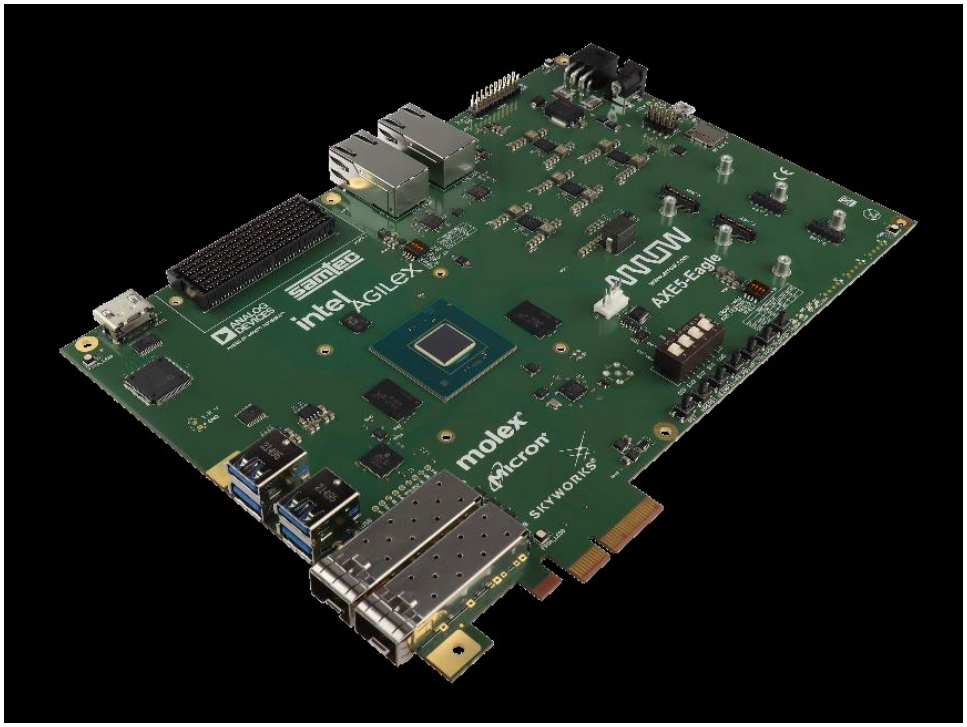

FIGURE 2 AXE-5 EAGLE BOARD

3. IDE (Integrated Development Environment) Support

The Intel Cyclone V FPGA is supported using the Intel ® Quartus Prime Lite Edition Design Software. The LITE edition is a free use IDE and is available for download from Intel ® web site located here: https://www.intel.com/content/www/us/en/software-kit/684216/intel-quartus-prime-lite-edition-design-software-version-21-1-for-windows.html (you can also choose your preferred version)

Along with the IDE it is highly encouraged users to download the Intel ® recommended documentation.

Documentation Links:

- Intel® Quartus® Prime Software User Guides
- Intel® FPGA Software Installation and Licensing Manual
- Intel® Quartus® Prime Software and Device Support Release Notes (PDF)

4. Memory Controller Support

EMxxLX is Everspin's latest Industrial STT MRAM supporting JESD251 Expanded Serial Peripheral Interface (xSPI). To properly support this new JEDEC standard an xSPI compatible memory controller is required. Synaptic Labs LLC MBMC (Multi-Bus Memory Controller) IP is used in this evaluation board.

The Memory Controller IP temporary license (.lic) file is provided by Synaptic Labs LLC. Link for requesting temporary license file is here: https://synaptic-labs.com/free-trial-request/

After contacting and receiving the temporary license file, follow all directions contained in the Synaptic guide for installing and configuring the Memory controller IP.

5. IDE Software Installation and Configuration

To program the FPGA with the correct image Quartus Prime IDE is used in conjunction with Synaptic Labs MBMC (Multi-Bus Memory Controller) IP. Locate the Quartus Prime IDE install file downloaded in section 3. Follow the installation instructions associated with the file. The user guide assumes default file location is used during the installation process.

6. Reading and Writing EMxxLX MRAM

Contained within the Synaptic user guide are instructions for reading and writing the EMxxLX device.

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Summary

This Evaluation platform user guide has been provided to give users the ability to evaluate Everspin's EMxxLX Industrial MRAM.

The detailed steps provide users the required download and installation instructions for the Integrated Development Environment (IDE), SW support packages, License files and USB programming tools. After proper configuration, the user can download the required FPGA .SOF and ELF files to test and evaluate EMxxLX industrial MRAM.

Revision History

Revision	Date	Description of change
1.0	November 06, 2024	Initial Release

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