Introduction

The EMxxLX family is the latest generation of ***PERSYST*** MRAM devices based on Everspin's STT (Spin-Transfer Torque) technology. It is a high-performance, multiple I/O, xSPI compatible MRAM device featuring a low pin count SPI bus interface with supported frequencies up to 200 Mhz.

Several system variables impact certain Industrial STT-MRAM characteristics. Specifically, temperature and data payload size impact Data Retention and Device endurance respectively.

This application note will focus on system and environmental variables that impact device endurance.

The information provided in this application note is specific to the Industrial STT-MRAM manufactured on the 28nm process node. Future generations of Industrial STT-MRAM will be manufactured on different process nodes with different data retention and endurance characteristics.

Contents

Endurance versus Ambient Temperature

The operational temperature can have a significant impact on EMxxLX device endurance modeling and real world performance.

For the EMxxLX extended temperature device the operational window of -40 to 105C will be discussed. All items discussed will be directly applicable to the EMxxLX Industrial and Commercial devices.

When discussing the temperature impact on Endurance, the workload must also be included. For this document the workload has two properties, a Read/Write Ratio and Payload size. The R/W ratio is the percentage of Reads vs Writes. Payload size is defined in the Payload and Data transfer section.

Operational temperature for this discussion is defined as the temperature where the EMxxLX device will perform the abundance of Read and Write cycles over the life of the device. From historical models most devices do not typically perform large workload operation in temperatures from -40 to -5 C ambient, but full device functionality is expected at these temperatures. Conversely from historical model's large workload operation is typically in the temperature range of 25C - 75C ambient.

Worst case operational temperature for EMxxLX devices is extreme cold environments for write operations. Conversely higher Ta operating temperatures is the ideal operating environment when discussing endurance.

To determine the maximum number of writes or 'endurance' of an individual cell, several factors are taken into consideration.

1) MTJ breakdown failure rates as a function of write cycles with temperature and voltage acceleration.
2) Process variation resulting in subsequent MTJ size and Resistance.
3) Weibull modeling incorporating max sigma process variation to determine worst case endurance performance for shipping devices.

Payload or Data Transfer size

The transfer size or data payload should be a factor for consideration when trying to maximize device endurance.

For the purpose of this application note, four transfer sizes will be discussed.

1. Full Chip 64Mbit or 8,388,608 Bytes
2. 1KByte or 1024 Bytes
3. ECC word or 32Byte access
4. 4 Byte access

The worst-case transfer size for most byte addressable memory is a 1 Byte accesses. In this scenario the 1 Byte of data is written to the same address space over the life of the application. If the application or usage model does require access sizes in the range of one or two bytes, there are some small recommendations outlined in the Extending Endurance consideration section. These recommendations ensure device endurance over the life of the system.

The ideal access pattern for device endurance is a uniform Device access pattern. This distributes the workload evenly across the full device address range.

If uniform device access is not ideal, certain patterns or workloads can ensure robust device endurance for the life of the part.

Workload and Use cases for End-of-Life endurance

The device use case is usually defined as a ratio of Read to Writes. For example, a R/W ratio of 50% is where 50% of device accesses are Reads and the other 50% of device accesses are Writes. From analysis of many workloads on MRAM devices a typical R/W ratio is 40/60. This is where 40% of the workload are Reads and the other 60% are Writes. We will use this workload to calculate the number of writes in a 10 Year Period. For increased accuracy of use case numbers 3 and 4, Chip Select de-assertion times have been included. With the relatively small transfer size the CS deselect time can have a significant impact on write times.

Use Case #1: Uniform writes across entire 64Mbit address space

1) 200Mbytes/s

2) 8,388,608 Bytes of a data space

3) 100 % writes across the device address space

(60 sec/min) (60 mins/hr)(24 hrs/day)(365.24 days) x 200 Mbytes/s

31,556,736 sec/year x 200,000,000 bytes/sec = 6,311,300,000,000,000 Bytes/Year

= 6,311,300,000,000,000 /8,388,608 = 752,365,589 writes/year

EMxxLX Endurance = 1E14 Writes/752,365,589 Writes/year

= 132K years

Use Case#2: Writes across 1024 Byte Address Space

6,311,300,000,000,000 /1024

6,163,378,906,250 Writes/Year

1E14/6,163,378,906,250

= 16 Years

Use Case #3: Writes across 32 Byte Address Space

6,311,300,000,000,000 /32

197,228,125,000,000 Writes/Year

1E14/197,100,000,000,000

= .507 + CS deselect time = .81 Years

= 295 Days

Use Case #4 : Writes across 4 Byte Address Space

6,311,300,000,000,000 Bytes/Yr /4 Bytes

1,577,825,000,000,000 Writes/Year

1E14/1,577,825,000,000,000

.063 Years + CS deselect time = .36 years

= 133 Days

As shown in the four use cases described above, device endurance can be significantly impacted by the amount of address space used.

Using the full 64Mbit addressable space uniformly allows for continuous writes > 100K years. Conversely writing to a small 4-byte address space will reach the endurance limit is 133 days of writing. It is expected that neither use case is typical but are provided to show the endurance impact of the address space used.

All 4 use cases provided were using 100% write workload, which is not a typical use case of 40% Reads and 60% Writes. Applying that workload to all 4 use cases above results in 40% increase in time. Taking use case 3, 32 Bytes of address space with 295 days of endurance would result in 118 additional days of write time. The total write time is increased to 413 days.

Extending Endurance considerations

To assist system designers and developers in ensuring robust device endurance, an example of payload and access optimization is included below.

As discussed earlier in the End-of-life use case scenarios, the best access pattern when considering endurance is full chip uniform access. When using this access, all temperature and endurance considerations are eliminated.

When full chip utilization is not feasible due to required use case scenario limitations, the 1024 Byte uniform access should be considered. Using 1024 Byte area of memory uniformly and consecutively will allow for > 16 years of continuous use.

To ensure uniform access, a small counter or incrementor can be implemented in software. This incrementor will allow for uniform memory access. An example of a standard C+ incrementor function is included below for reference.

Example Incrementor function:

```
// CPP program to demonstrate special
// case of post increment operator
#include <iostream>
using namespace std;

int main()
{

    int x = 10;

    cout << "Value of x before post-incrementing";

    cout << "\nx = " << x;

    x = x++;

    cout << "\nValue of x after post-incrementing";

    // Value of a will not change
    cout << "\nx = " << x;

    return 0;
```

Conclusion

The EMxxLX family of devices have very robust endurance ratings over the life of the device. Certain considerations can help ensure End-of-Life device endurance under the worst-case workload and temperature environments.

This application note has provided the tools necessary to ensure robust device operation over the life of the device.

Revision History

Revision	Date	Description
1.0	June, 2024	Initial Release

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