Introduction

The EMxxLX is the latest generation of MRAM devices based on Everspin's STT (Spin-Transfer Torque) technology. It is a high-performance, multiple I/O SPI compatible MRAM device featuring a low pin count SPI bus interface with supported frequencies up to 200 Mhz. When the EMxxLX is configured for DTR operation with a clock speed of 200Mhz, transfer rates of 400MBps are achievable.

When utilizing higher bus speeds, it is desirable to optimize or tune the bus for increased data integrity and robustness. Tuning is described as locating or determining the optimal placement of Receive sample point timing. This tuning operation is accomplished by utilizing the TDP (Tuning Data Pattern) feature integrated into EMxxLX devices. This document will describe the required device settings and logical order of operations to accomplish the receiver tuning.

It is assumed the reader has full access to EMxxLX data sheet as certain registers and functions of the device are referenced throughout this document.

Contents

I/O Mode and DS (Data Strobe) Configuration

TDP can be used with or without the DS (Data Strobe) functionality. The DS functionality is supported in all operating modes SPI, DSPI, QSP and OSPI. Device I/O mode configuration is controlled by Nonvolatile and Volatile configuration register 0, Bits [7:0].

After POR the devices operational I/O settings are loaded from Nonvolatile configuration space. These settings may be overwritten during device operation by utilizing the Write Volatile Configuration Register command.

Nonvolatile Configuration Register 0				
Address	**0x00_0000**			
Bit	**Op**	**Name**	**Settings**	**Description**
7:0	RW	I/O Mode	1111_1111 (0xFF) 1101_1111 (0xDF) 1111_1101 (0xFD) 1101_1101 (0xDD) 1111_1011 (0xFB) 1101_1011 (0xDB) 1110_1011 (0xEB) 1100_1011 (0xCB) 1110_0111 (0xE7) 1100_0111 (0xC7) 1011_0111 (0xB7) 1001_0111 (0x97) Others	SPI with DS (default) SPI w/o DS Dual with DS Dual w/o DS Quad with DS Quad w/o DS Quad DTR with DS Quad DTR w/o DS Octal DTR with DS Octal DTR w/o DS Octal with DS Octal w/o DS SPI with DS (same as default)

Volatile Configuration Register 0				
Address	**0x00_0000**			
Bit	**Op**	**Name**	**Settings**	**Description**
7:0	RW	I/O Mode	1111_1111 (0xFF) 1101_1111 (0xDF) 1111_1101 (0xFD) 1101_1101 (0xDD) 1111_1011 (0xFB) 1101_1011 (0xDB) 1110_1011 (0xEB) 1100_1011 (0xCB) 1110_0111 (0xE7) 1100_0111 (0xC7) 1011_0111 (0xB7) 1001_0111 (0x97) Others	SPI with DS (default) SPI w/o DS Dual with DS Dual w/o DS Quad with DS Quad w/o DS Quad DTR with DS Quad DTR w/o DS Octal DTR with DS Octal DTR w/o DS Octal with DS Octal w/o DS SPI with DS (same as default)

TDP Default Data Sequence

The TDP default data sequence is loaded after POR into TDP register space. The TDP consist of 64 Bytes of data defined below in Table 1.

Address	0x0000 - 0x0020		Address	0x001F - 0x003F	
Byte Address	Name	Settings	Byte Address	Name	Settings
0x00	TDP Byte 0	0xDE	0x1F	TDP Byte 31	0xFF
0x01	TDP Byte 1	0x7B	0x20	TDP Byte 32	0xEF
0x02	TDP Byte 2	0x7F	0x21	TDP Byte 33	0xBD
0x03	TDP Byte 3	0xF7	0x22	TDP Byte 34	0xF7
0x04	TDP Byte 4	0xFF	0x23	TDP Byte 35	0x77
0x05	TDP Byte 5	0xF7	0x24	TDP Byte 36	0xFF
0x06	TDP Byte 6	0xFF	0x25	TDP Byte 37	0x7F
0x07	TDP Byte 7	0xBB	0x26	TDP Byte 38	0xFF
0x08	TDP Byte 8	0xFF	0x27	TDP Byte 39	0xBF
0x09	TDP Byte 9	0xBF	0x28	TDP Byte 40	0xFB
0x0A	TDP Byte 10	0xFF	0x29	TDP Byte 41	0xFF
0x0B	TDP Byte 11	0xDF	0x2A	TDP Byte 42	0xFB
0x0C	TDP Byte 12	0xFD	0x2B	TDP Byte 43	0xFF
0x0D	TDP Byte 13	0xFF	0x2C	TDP Byte 44	0xDD
0x0E	TDP Byte 14	0xFD	0x2D	TDP Byte 45	0xFF
0x0F	TDP Byte 15	0xFF	0x2E	TDP Byte 46	0xDF
0x10	TDP Byte 16	0xEE	0x2F	TDP Byte 47	0xFF
0x11	TDP Byte 17	0xFF	0x30	TDP Byte 48	0xEF
0x12	TDP Byte 18	0xFF	0x31	TDP Byte 49	0xFE
0x13	TDP Byte 19	0xFE	0x32	TDP Byte 50	0xFF
0x14	TDP Byte 20	0xCF	0x33	TDP Byte 51	0xFE
0x15	TDP Byte 21	0xCC	0x34	TDP Byte 52	0xFF
0x16	TDP Byte 22	0x33	0x35	TDP Byte 53	0xCC
0x17	TDP Byte 23	0xCC	0x36	TDP Byte 54	0x3C
0x18	TDP Byte 24	0x3C	0x37	TDP Byte 55	0xC3
0x19	TDP Byte 25	0xCC	0x38	TDP Byte 56	0xCC
0x1A	TDP Byte 26	0xFC	0x39	TDP Byte 57	0xC3
0x1B	TDP Byte 27	0x0F	0x3A	TDP Byte 58	0xCC
0x1C	TDP Byte 28	0xF0	0x3B	TDP Byte 59	0xFF
0x1D	TDP Byte 29	0xFF	0x3C	TDP Byte 60	0x00
0x1E	TDP Byte 30	0xF0	0x3D	TDP Byte 61	0xFF
0x1F	TDP Byte 31	0xFF	0x3E	TDP Byte 62	0x0F
0x20	TDP Byte 32	0xEF	0x3F	TDP Byte 63	0xFF

TABLE 1 TDP DATA STRUCTURE

Programing Custom TDP

TDP can be programmed with a custom data pattern based on user preference. The Device is configured for desired I/O Mode operation prior to writing TDP data pattern.

TDP data pattern is written using the TDP Write command code 0xF0.

TDP write sequence is defined in Figure 1.

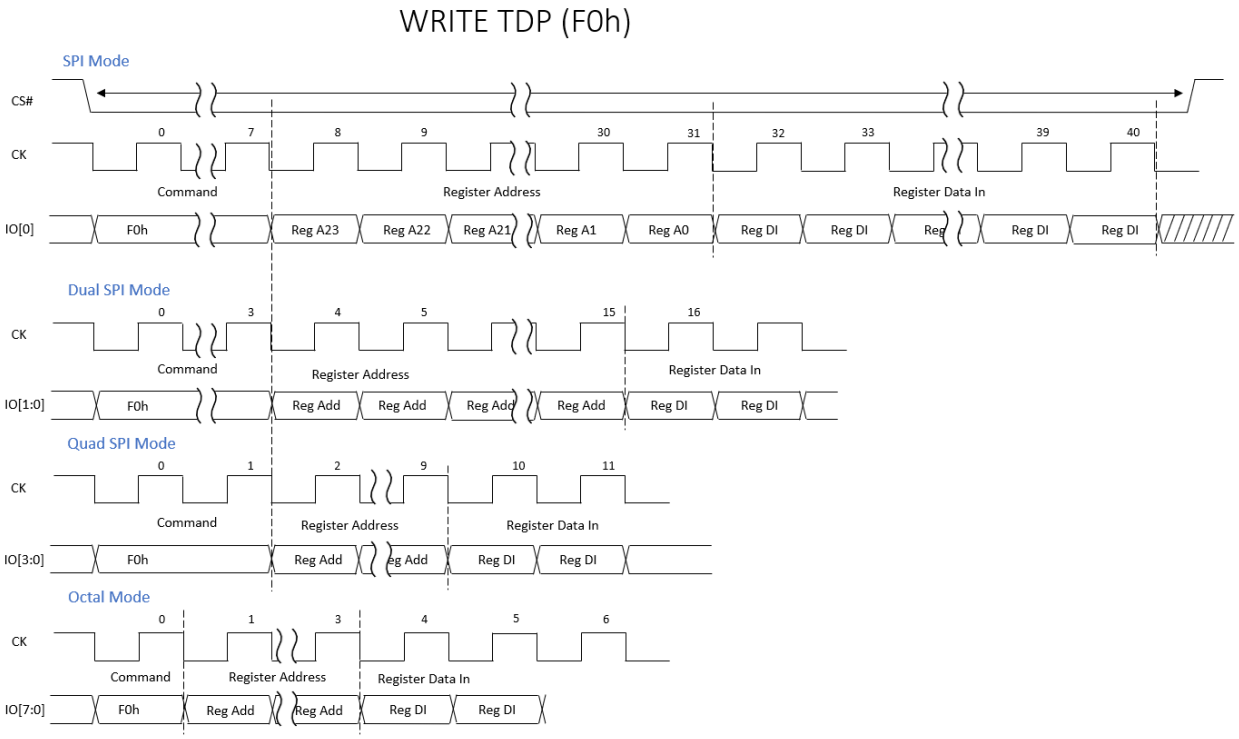

FIGURE 1 WRITE TDP TIMING DIAGRAM

TDP Read Operation

TDP read operation is similar in function to FAST READ. Reading the TDP data structure is accomplished utilizing the TDP Read command (0xF1)

TDP read sequence is defined in Figure 2 below.

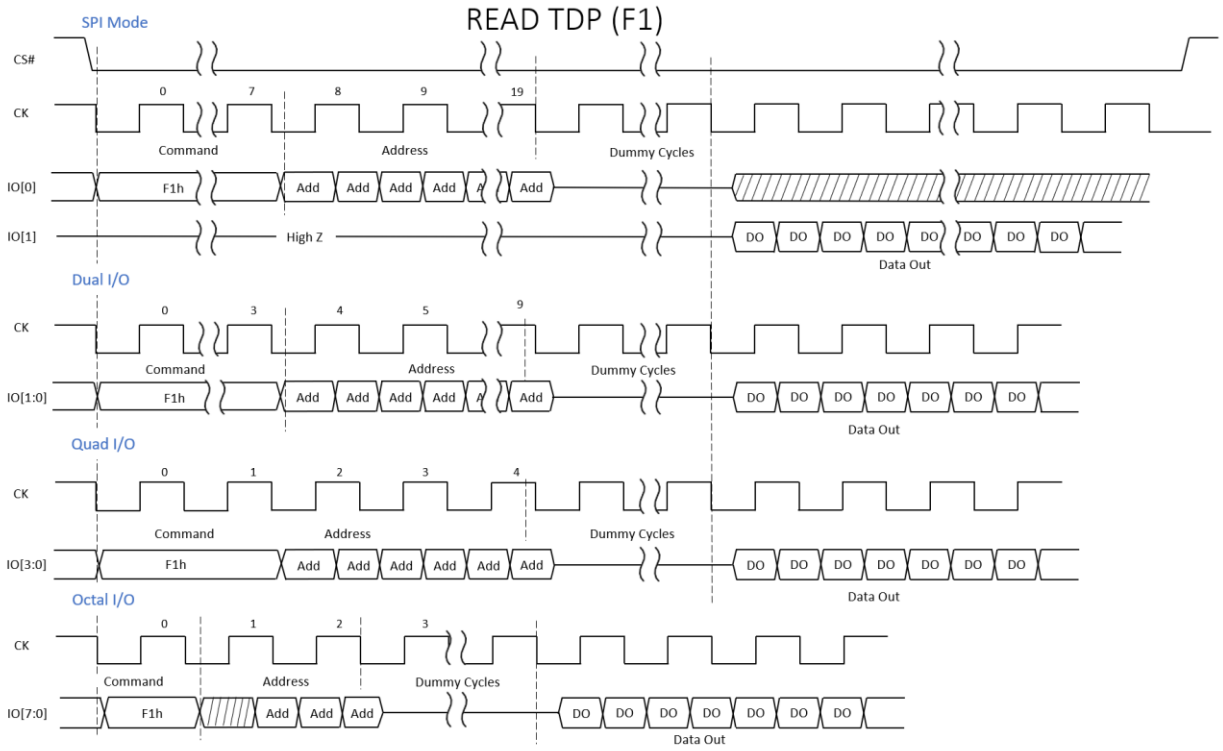

FIGURE 2 READ TDP TIMING DIAGRAM

DS (Data Strobe) Delay Settings

To allow flexible tuning of the receiver sample point during reads, EMxxLX supports a feature allowing the controller to delay DS in relation to the data. Using the TDP and logical tuning sequence the optimal sample point using the DS can be achieved. By default, the initial delay is set to 0 so data and DS will be phase aligned.

The DS delay is controlled with the DS delay settings in Nonvolatile Configuration Register, bits [3:0].

TDP Logical Sequence of Operation

For proper TDP operation the following sequence of events is recommended. Please refer to TDP logical sequence flow chart Figure 3.

1) Configure the device for desired interface speed and I/O mode of operation. Supported modes are SPI, Dual SPI, Quad SPI and Octal SPI.
    a. All SPI modes can be configured with/without DS Operation.

b. For TDP tuning sequence it is recommended to configure the device for DS operation. The DS will be used as initial qualifier for determining optimal timing of the Receiver sample point.
c. It is recommended to use lower Host Clock speeds for initial TDP structure read out.
d. Supported frequencies are defined in Section 5.8 of product data sheet.

2) Read TDP data pattern into a predefined 512 Byte Host side structure.
   a. The host side data structure will hold the TDP data used during tuning process
   b. During Read TDP operations, when configured for DS operation, the DS will be phase aligned and closely coupled with Data out.
   c. After initial TDP readout set Host Clock to desired speed of operation.
   d. Follow TDP logical flow chart steps in Figure 3 for determining optimal Data Strobe placement.
   e. Once the optimal strobe placement is determined use the required Data Strobe Delay settings to place the Data Strobe in the optimal desired location.

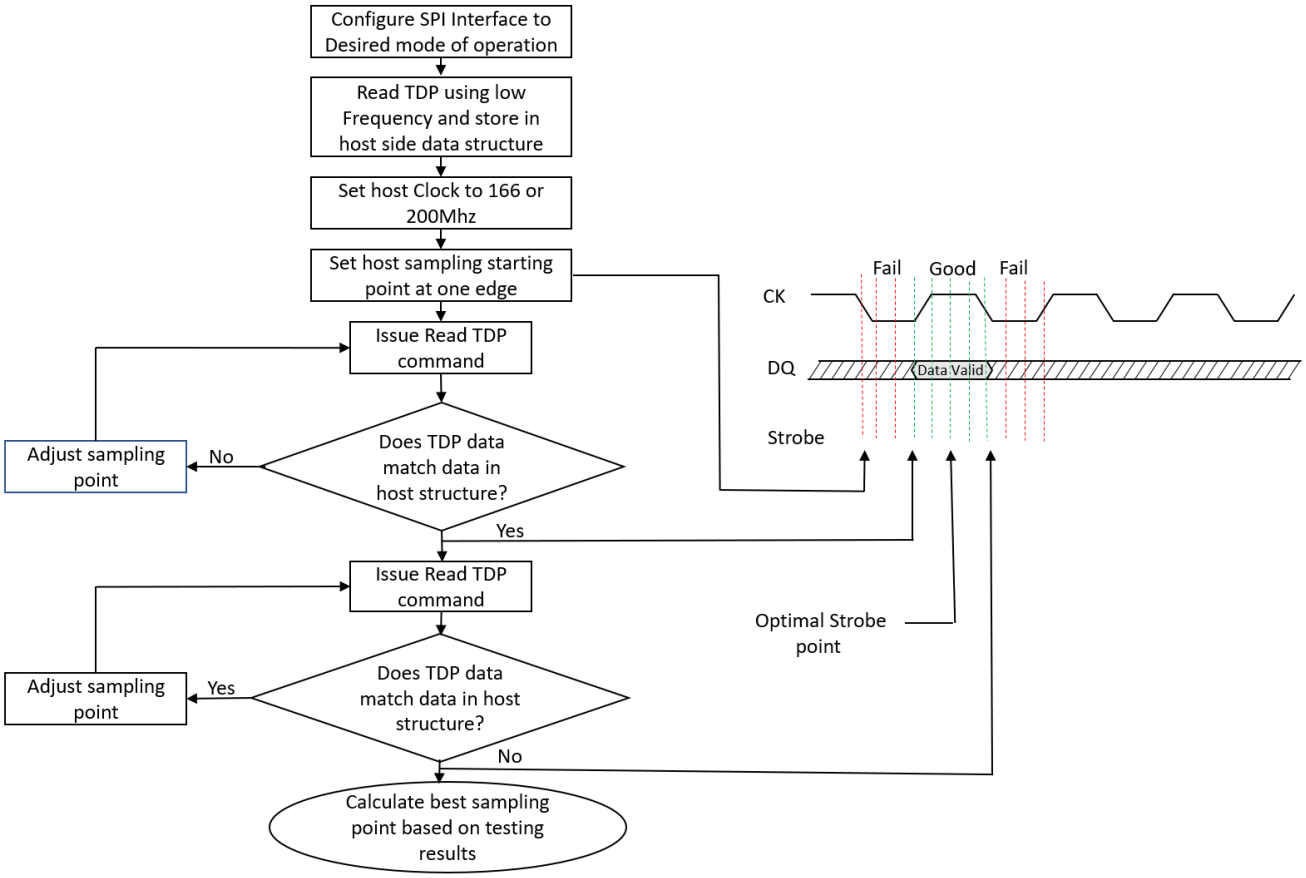

FIGURE 3 TDP LOGICAL FLOW CHART

Conclusion

Everspin's latest generation of STT MRAM device, the EMxxLX, offers design flexibility and speed with its latest xSPI implementation. When configured for DTR with Data Strobe operation, 400Mbytes/sec throughput can be achieved. With higher bus speeds, care must be taken to ensure proper tuning and placement of the Data Strobe.

The TDP data pattern and subsequent tuning operation allow for the proper placement and timing of the Data Strobe.

Revision History

Revision	Date	Description of change
1.0	June 17, 2022	Initial Release
1.1	October 22, 2022	Updated Interrupt Mask and Status Register description.

Contact Information:

Author: Daniel Symalla

Director of System Applications

WW Sales Group

How to Reach Us:

www.everspin.com

E-Mail:

support@everspin.com

orders@everspin.com

sales@everspin.com

USA/Canada/South and Central America

Everspin Technologies

5670 W. Chandler Road, Suite 100

Chandler, Arizona 85226

+1-877-347-MRAM (6726)

+1-480-347-1111

Europe, Middle East and Africa

support.europe@everspin.com

Japan

support.japan@everspin.com

Asia Pacific

support.asia@everspin.com

Everspin Technologies, Inc.