Introduction

The EMxxLX/LXB is the latest generation of MRAM devices based on Everspin's Industrial STT (Spin-Transfer Torque) technology. It is a high-performance, multiple I/O, SPI compatible MRAM device featuring a low pin count SPI bus interface with supported frequencies up to 200 Mhz. When the EMxxLX/LXB is configured for DTR operation with a clock speed of 200Mhz, transfer rates of 400MBps are achievable.

The device state cannot be guaranteed after a solder reflow operation, hence a full device initialization and configuration is required. This document will outline the required steps, sequence of operations, and register settings required to have the EMxxLX/LXB in a fully functional and ready state.

Please refer to the EMxxLX/LXB data sheets for additional reference as certain registers and functions of the device are referenced throughout this document.

Contents

List of Figures and Tables

1. Device Initialization, Power Cycle, System Resets and Recovery logical flows

For device initialization, Power On/Reset and recovery, an order of operations or 'logical flow' has been developed. This flow is designed to assist the user in defining the logical sequence and steps required for device initialization and recovery. Determining when the recovery flow should be initiated or is required is left to the system designers. It is assumed some level of end-to-end data protection scheme will be implemented. This protection scheme will be the first to identify undefined or unexpected system behavior.

It is intended that host controllers follow the Device Initialization flow for first time power-on after device manufacturing. The Device Power On or Device Reset Flow will be used for subsequent power on or reset events.

Determining when the recovery process should be done is left to the system designers. General reasons to consider running the recovery process would be:

- Inability to communicate with the memory device.
  - This could come from loss of synchronization between the system memory controller and the memory via a reset or power lost to one but not the other device.
  - A failure of power-on or other reset initialization of the memory xSPI logic.
  - This communication failure may be detected by a system watchdog time out or by boot or diagnostic code, executing from a different system memory resource, that is used to verify data integrity of the memory contents before normal system operation begins.
- Detection of a Power-on error as shown in the Flag Status Register, bit 2, when set to 1.
- Detection of data errors in the non-volatile configuration registers, main memory array, or OTP memory array.

It is assumed some type of data integrity monitoring scheme will be implemented by the system, such as a checksum or CRC on the memory arrays. This protection scheme will likely be the first to identify memory content errors.

Device Initialization, Power On/Reset and recovery flows are defined in Figures 1, 2 and 3 below.

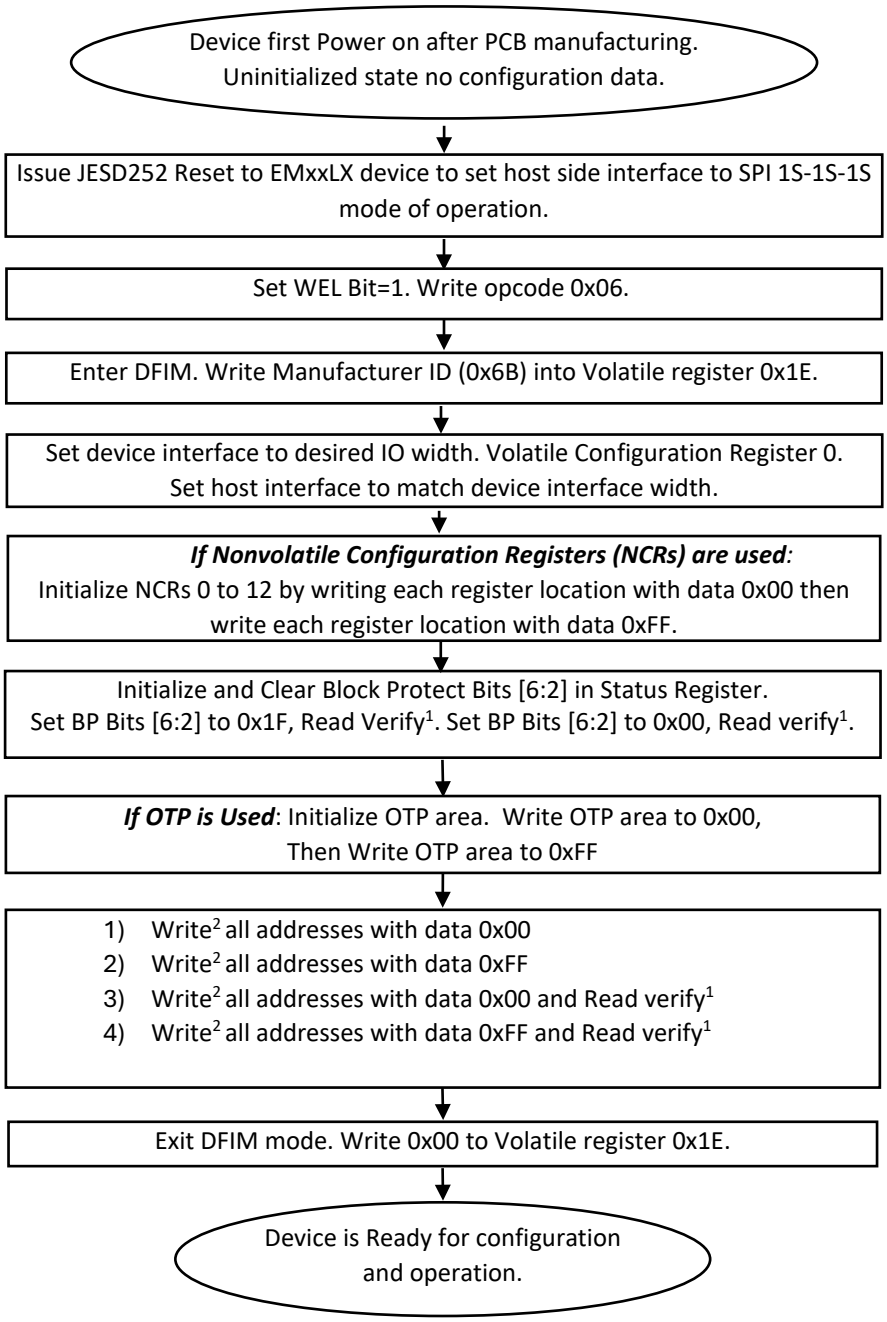


FIGURE 1 DEVICE INITIALIZATION FLOW

Note 1: Read verify is an optional step to confirm data is in correct state to verify initialization sequence was properly applied.

Note 2: Erase/Bulk Chip (Opcodes 0xC7 and 0x60) or other Erase commands may be used in place of write commands. If using Erase commands, set data state for Erase Operation in Volatile Configuration Register 8, bit 7, to 0 to write 0x00 and set Erase data state to 1 to write 0xFF.

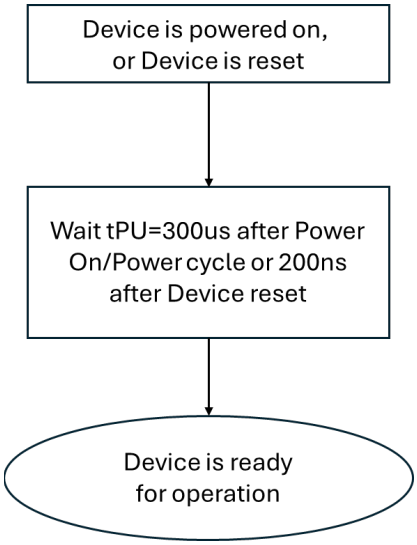


FIGURE 2 DEVICE POWER ON/RESET FLOW

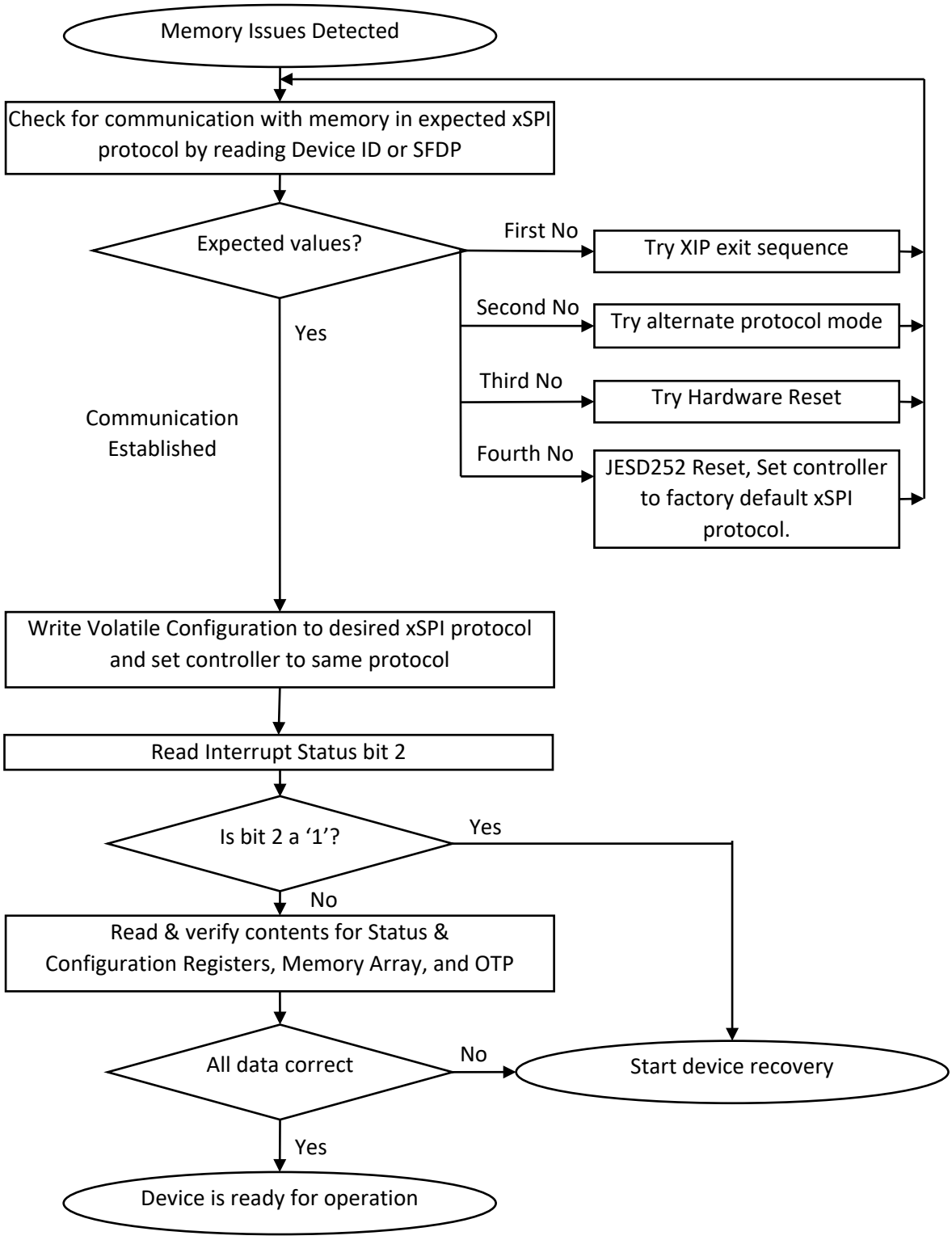


FIGURE 3 DEVICE RECOVERY FLOW PART 1

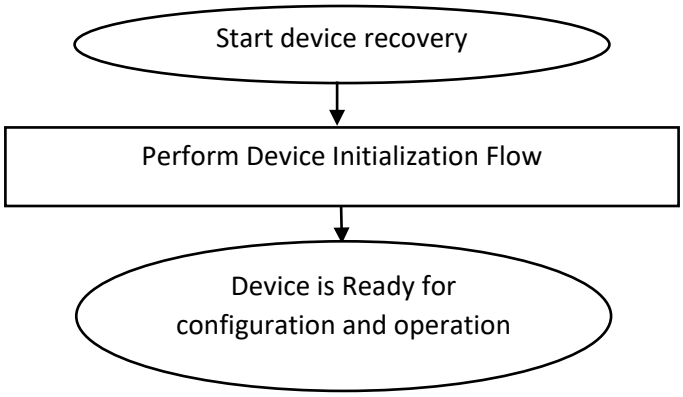


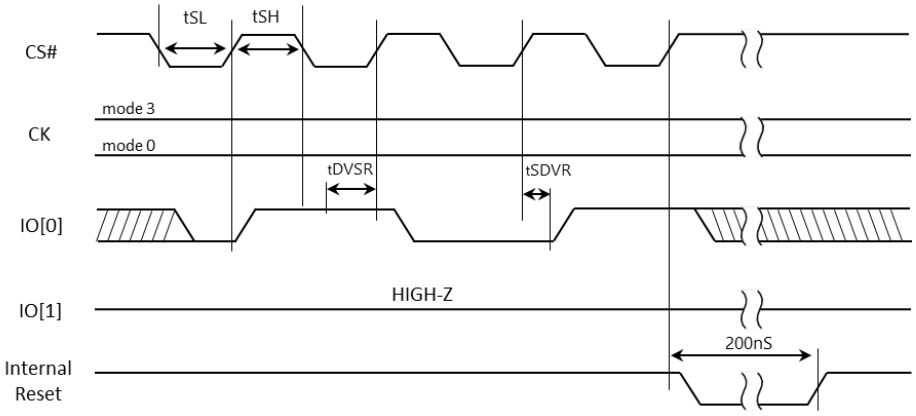
FIGURE 4 DEVICE RECOVERY FLOW PART 2

2. SPI Interface configuration

After manufacturing and reflow operations, device register settings and array contents are not defined. The EMxxLX/LXB interface default configuration after a solder reflow operation or JEDEC reset is SPI 1S-1S-1S mode of operation. All initial commands must use this format until the interface is configured for desired mode of operation.

3. JEDEC Reset Considerations

Not all MCU controllers natively support JESD252 Signal reset sequence. In this scenario it is recommended customers investigate the GPIO remapping capabilities of the MCU controller used in the design. In many modern MCU it is possible to remap the current SPI interface signals as GPIO. If possible, remap CS#, CK, IO 0:1 as GPIO signals. Using the logic control capabilities of the GPIO signals perform the Signal Reset sequence outlined in Figure 5.



Parameter	Symbol	Min	Max	Units
CS# high time	tSL	500	-	ns
CS# high time	tSH	500	-	ns
Setup time data to CS# for Reset	tDVSR	5	-	ns
Hold time data to CS# for Reset	tSDVR	5	-	ns

FIGURE 5 JESD252 RESET WITH SIGNAL SEQUENCE

4. Nonvolatile Configuration Settings

EMxxLX/LXB Nonvolatile configuration registers are used to store the device configuration state. The Nonvolatile Configuration registers overwrite Internal Configuration Registers after Power-on or after a device reset. The user can change the default configuration at power up by using the Write Nonvolatile Configuration Register. Please refer to EMxxLX/LXB product data sheet for full register description and bit definitions. A brief summary of the Nonvolatile configuration registers is provided below in Table 1.

Nonvolatile Configuration Register	Address	Width	Functional Summary
Register 0	0x0000	8 bit	I/O Mode settings
Register 1	0x0001	8 bit	Dummy Cycle Configuration
Register 2	0x0002	8 bit	Reserved
Register 3	0x0003	8 bit	I/0 Driver Strength
Register 4	0x0004	8 bit	DS delay
Register 5	0x0005	8 bit	Address Mode
Register 6	0x0006	8 bit	XIP Configuration
Register 7	0x0007	8 bit	Wrap Configuration
Register 8	0x0008	8 bit	Erase, Reset, Write mode

TABLE 1 NONVOLATILE CONFIGURATION REGISTERS

5. Volatile Configuration Register Settings

Volatile configuration registers are used to overwrite the device configuration during operation or run time. Register download is executed after a Write Volatile Configuration Register Command. This command will overwrite configuration settings in Internal Configuration Registers.

Nonvolatile Configuration Register	Address	Width	Functional Summary
Register 0	0x0000	8 bit	I/O Mode settings
Register 1	0x0001	8 bit	Dummy Cycle Configuration
Register 2	0x0002	8 bit	Reserved
Register 3	0x0003	8 bit	I/0 Driver Strength
Register 4	0x0004	8 bit	DS delay
Register 5	0x0005	8 bit	Address Mode
Register 6	0x0006	8 bit	XIP Configuration
Register 7	0x0007	8 bit	Wrap Configuration
Register 8	0x0008	8 bit	Erase, Reset, Write mode

TABLE 2 VOLATILE CONFIGURATION REGISTERS

6. Status Register

Read Status Register or Write Status Register commands are used to read from or write to the Status Register bits, respectively. When the status register enable/disable bit (bit 7) is set to 1 and WP# is driven LOW, the status register nonvolatile bits become read-only and the Write Status Register operation will not execute. This hardware-protected mode is exited by driving WP# high.

For array initialization and recovery, the BP bits [6:2] must be cleared or set to ‘0’. This disables block protection and defines all areas of the array as writable.

7. Flag Status Register

The Read Flag Status Register command is used to read the Flag status register bits. Flag status registers bits are volatile and are reset to zero on power-up They are set and reset automatically by the internal controller. Error bits must be cleared through the Clear Status Register command.

Flag Status Register				
Bit	**Name**	**Settings**	**Description**	**Type**
0	Addressing	0 = 3-byte addressing 1 = 4-byte addressing	Indicates whether 3-byte or 4-byte address mode is enabled.	Status
1	Protection	0 = Clear 1 = Failure or Protection Error	Indicates whether an Erase or Program operation has attempted to modify the protected array sector as configured by Block Protection, or whether a OTP Write operation has attempted to access the locked OTP space.	Error
2	Reserved			
3	CRC	0 = Clear 1 = Failure	Indicates that the Computed CRC did not match the user provided CRC Code.	Error
4	Write (Program)	0 = Clear 1 = Failure or Protection Error	Indicates whether a Program operation has succeeded or failed. A PROGRAM or OTP Write operation will fail if WREN is not set or attempting to PROGRAM a region that has Block Protection enabled.	Error
5	Erase	0 = Clear 1 = Failure or Protection Error	Indicates whether an Erase operation has succeeded or failed. An Erase operation will fail if WREN is not set.	Error
6	Reserved			
7	Write (Program) or Erase	0 = Busy 1 = Ready	Indicates whether one of the following command cycles is in progress: Write Status Register, Write Nonvolatile Configuration Register, Write (Program), Erase, or CRC Check.	Status

TABLE 3 FLAG STATUS REGISTER

8. Interrupt Status Register

The Interrupt Mask and Status registers are used together to provide the status of certain operations or indicate errors in particular operations as shown in the tables below. The mask register provides the option to receive an interrupt signal on the INT# pin. The INT# is available on the 24-ball BGA, ball A5 but is not available on the 8-DFN package. Configuration errors, CRC completion and Erase completion are the operations that generate a status bit. The Interrupt registers are accessed with the Read Volatile Configuration Register and Write Volatile Configuration Register commands.

Interrupt Mask					
Address	**0x000F**				
Bit	**Op**	**Name**	**Settings**	**Description**	**Notes**
7:2	RO	Reserved	0		
1	RW	CRC Done	0 = Masked (default) 1 = Interrupt enabled	Enable interrupt on CRC Check Done	
0	RW	Erase Done	0 = Masked (default) 1 = Interrupt enabled	Enable interrupt on Erase Done 1=Masked - no interrupt is generated	

Interrupt Status					
Address	**0x0010**				
Bit	**Op**	**Name**	**Settings**	**Description**	**Notes**
7:3	RO	Reserved	0		
2	RW1C	Power On Error	0 = No error 1 = Error	Read, Write 1 to Clear, Power on error	1
1	RW1C	CRC Done	0 = Not done (Reset Value) 1 = Done	Read, Write 1 to Clear	
0	RW1C	Erase Done	0 = Note done (Reset Value) 1 = Done	Read, Write 1 to Clear	

TABLE 4 INTERRUPT FLAG AND STATUS

Note 1. Bit 2 does not get reset with a hardware reset.

9. Considerations for Extreme Temperature Exposure

The DFIM factory initialization procedure is intended to be a one-time event after soldering the EMxxLX to the PCB, i.e. after solder reflow, during system setup.

If there are any subsequent solder reflow or extreme temperature exposures, the DFIM factory initialization procedure will need to be completed prior to device operation. In this case, extreme temperature exposure is 125^{o}C for one hour or more.

10. OTP Considerations

A dedicated area of 256 bytes outside of the memory array is provided to allow specific user information to be stored on a non-volatile basis. This area is controlled using the OTP control byte and Volatile Configuration register 8, bit 2. Please refer to EMxxLX/LXB data sheet section 14 for OTP operation and Control Byte specifics and, Section 5.5 for Nonvolatile Configuration Register definitions.

11. Configuration Save State and verification

After the device is configured for desired operation, it is recommended to save all Volatile, Nonvolatile and Status Registers to a host side structure. This structure will be used for comparison during the Initialization and Recovery flow to ensure accuracy of device initialization.

12. Array Initialization Steps

For proper functional operation of the EMxxLX/LXB, a memory Array initialization is required. This section defines the steps to properly initialize and program the memory array.

1) Set host side interface to SPI mode of operation.
2) Set WEL Bit=1.
3) Write Device ID to Volatile register 0x1E to enter DFIM (Device Factory Initialization Mode)
4) Initialize Non-Volatile registers [C:0] *(if used)*. Write each register location to 0x00 then Write each register location to 0xFF.
5) Initialize and Clear Block Protect Bits [6:2] in Status Register. Set BP Bits [6:2] to 0x1F, Read Verify. Set BP Bits [6:2] to 0x00, Read verify.
6) ***If OTP is Used***: Initialize OTP area. Write OTP area to 0x00.Write OTP area to 0xFF
7) Write [1] all addresses 0x00
8) Write[1] all addresses 0xFF
9) Write[1] all addresses 0x00 and read verify[2]

10) Write[1] all addresses 0xFF and read verify[2]
11) Write 0x00 to Volatile register 0x1E to exit DFIM mode.
12) Device is ready for operation.

Note 1. Erase/Bulk Chip or Erase commands may be used in place of write commands.

Note 2. Read verify is an optional step to confirm data is in correct state and verify device initialization was performed properly.

13. Device Initialization Command sequence

To assist developers in generating the code sequence for device initialization a sample command sequence has been developed below. Please refer to proper timing and data sequence diagrams in EMxxLX/LXB data sheet for details.

1) Set host controller to SPI mode. Please refer to documentation provided for the host controller.
2) Set WEL (Write Enable Latch) Bit 1 and Write Device ID in Volatile register 0x1E to enter DFIM.
    a. Command = 06h
    b. Command = 81h, Register Address, Register Data In
3) Set Device interface to desired IO width.
    a. Command = 81h Register Address, Register Data In
4) Write Non-Volatile Registers if used.
    a. Command = B1h Register Address, Register Data In
5) Initialize and Clear Block Protect Bits [6:2] in Status Register. Set BP Bits [6:2] to 0x1F, Read Verify. Set BP Bits [6:2] to 0x00, Read verify.
    a. Status Register Write Command = 01h
    b. Read Status Register Command = 05h
6) If OTP is Used: Initialize OTP area. Write OTP area to 0x00. Write OTP area to 0xFF
    a. Write OTP Command = 42h, Address, Data
7) Write[1] all addresses 0x00.
    a. Command: Refer to Write Operations section of EMxxLX Data sheet.
8) Write[1] all addresses 0xFF.
    a. Command: Refer to Write Operations section of EMxxLX Data sheet.
9) Write[1] all addresses 0x00 and read verify.
    a. Command: Refer to Write Operations section of EMxxLX Data sheet
    b. Command: Refer to Read Operations section of EMxxLX Data Sheet.
10) Write[1]all addresses 0xFF and read verify.
    a. Command: Refer to Write Operations section of EMxxLX Data sheet
    b. Command: Refer to Read Operations section of EMxxLX Data Sheet.
11) Write 0x00 to Volatile register 0x1E to exit DFIM mode
    a. Command = 81h, Address = 0x1Eh, Register data = 0x00h
12) Device is ready for operation.

Note1. Erase/Bulk Chip or Erase commands may be used in place of write commands.

14. Undefined or Unexpected device operation

In the event of device exposure to magnetic fields exceeding the immunity specification or extreme temperatures identified in section 9, the device operation can become undefined. Host side data integrity schemes are expected to alert the system when this event occurs. If this event is detected refer to device recovery flow.

Conclusion

Everspin's latest generation of STT MRAM device EMxxLX/LXB offers design flexibility and speed with JEDEC standard xSPI implementation. To ensure proper device operation after manufacturing and solder reflow, the device must be properly initialized. Following the sequence and steps outlined in this document will ensure the device operates in accordance with the specification outlined in the product data sheet.

Revision History

Revision	Date	Description of change
1.0	April 7, 2022	Initial Release
1.1	June 8, 2022	Added state to recovery flow to clear interrupt status bit [2] Added new section: Device Initialization Command sequence
1.2	August 1, 2022	Updated Device recovery flow
1.3	August 24, 2022	Added JEDEC Reset Considerations section Update Device Recovery flows
1.4	Oct 5, 2022	Added JESD252 Reset to Initialization Flow Updated device naming convention to EMxxLX/LXB
1.5	March 5, 2023	Updated Command sequence step with Write Enable (06h)
1.6	April 11, 2023	Updated naming convention to add EMxxLX/LXB
1.7	February 26, 2024	Updated initialization flow to enter DFIM earlier in logical flow. Updated device initialization command sequence to follow updated logical flow. Added section 9 Considerations for Extreme Temperature exposure
1.8	March 15, 2024	Updated Device Initialization flow chart Figure 1. Updated Array Initialization steps section. Updated Device Initialization command sequence section 13
1.9	May 10, 2024	Updated Device Initialization Flow Chart Figure 1 and Figure 2. Updated Device Initialization command sequence section 13. Added clarifications to section 14. Updated Fig 5. JEDEC reset diagram and timings

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