24-Ball BGA Packages

24-Ball BGA 6x8mm

- Compliant with RoHS, REACH regulations and practices.
- Contains no Red Phosphorus.
- Lead Free.
- Assembly with a JEDEC standard reflow profile.
- Compatible with similar low-power SRAM and other nonvolatile RAM products

Contents

Compliance with Environmental Regulations and Directives

Environment	Statement Summary	Download Full Statement
RoHS	Everspin Technologies, Inc. MRAM products comply with RoHS Directive 2002/95/EC.	Full RoHS Compliance Statement
REACH	Under the definition of the REACH regulations EC1907/2006, Everspin Technologies is a producer of "articles". REACH requires article suppliers to inform recipients if an article contains a Substance of Very High Concern (SVHC) in excess of 0.1% by weight. Everspin products do not contain any of these SVHC in excess of 0.1% by weight.	Full REACH Statement
Red Phosphorus	Everspin Technologies, Inc. MRAM products do not contain Red Phosphorus CAS# 7723-14-0 as an intentional additive.	Full Red Phosphorus Statement
Environmental and Humanitarian Compliance	Materials from Conflict Regions Statement	Full Statement
	EICCeSI Environmental and Humanitarian Compliance Form	Form

Multiple Reflow Cycles and Moisture Resistance

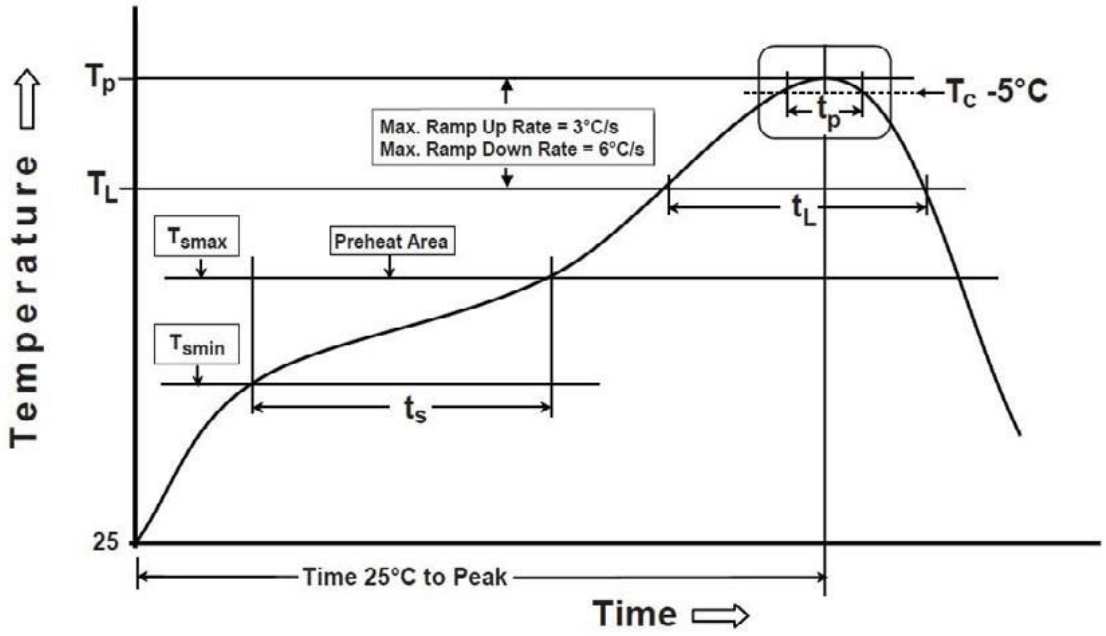
All Everspin packages are qualified by the procedure defined in IPC/JEDEC joint specification IPC/JEDEC J-STD-020D.1. They are guaranteed to withstand up to three reflow cycles without permanent damage, pro- vided the conditions for the rated moisture resistance level for the part are observed prior to reflow.

Everspin parts are generally rated for MSL Level 3. Exceptions may exist and are noted in their respective data sheet. Please the check the latest individual product data sheet to confirm the rated MSL for the product.

Recommended Reflow Temperatures and Timing – All Packages

Everspin products can be assembled using a standard reflow profile. The profile below is based on IPC/ JEDEC J-STD-020D.1.

FIGURE 1 - RECOMMENDED REFLOW PROFILE _ ALL PACKAGES



Profile Step	Parameter	Symbol	Time/Temp	Unit
Preheat / Soak	Temperature minimum	T_{SMIN}	150	°C
	Temperature maximum	T_{SMAX}	200	°C
	Soak Time	t_S	60 - 120	Seconds
Ramp Up	Rate from T_L to T_P	T_L to T_P	3° / Sec Max	° / Sec
	25°C to T_P		8 minutes max	Minutes
Reflow	Liquidous Temperature	T_L	217	°C
	Time Above T_L		60 - 150	Seconds
	Peak Package Body Temperature	T_P	260	°C
	Time T_C is within 5° of T_P		30	Seconds
Ramp Down	Rate from T_P to T_L	T_P to T_L	6° / Sec Max	° / Sec

Thermal Resistances

TABLE 1 – THERMAL RESISTANCE MR10Q010 6X8 MM 24-BGA

T_A (°C)	T_J (°C)		Θ_{JA} (°C/W)		Ψ_{JT} (°C/W)	Θ_{JB} (°C/W)
	0 m/s	1 m/s	0 m/s	1 m/s		
70	94.6	92.8	68.3	63.3	1.6	47.2

TABLE 2 - THERMAL RESISTANCE EMXXLX 6X8MM24-BGA

Mode	Package	Die Stack	Ta (C)	Θ_{JA} (C/W)		Θ_{JB} (C/W)	Θ_{JC} (C/W)	Ψ_{JT} (C/W)	
				0 m/s	1 m/s			0 m/s	1 m/s
XSPI	BGA	x1	25	65.3	52.8	46.6	14.4	0.7	1.6
XSPI	BGA	X2	25	53.0	43.1	34.3	7.9	0.6	2.7

Notes:

1. Θ_{JB} value assumes 4-layer PCB.
2. Ψ is a thermal characterization factor indicating the temperature rise between package top and the device junction. See JESD51-2.

Thermal Calculations

Designers may require different thermal numbers for specific models or environments. Figure 2 below depicts the JEDEC thermal resistances of typical packages. Using the thermal resistances and power provided in device specific data sheet, and using industry standard equations, the desired thermal variable can be calculated. Figure 3 depicts an example calculation using Ta to calculate Tj.

FIGURE 2 - JEDEC PCB THERMAL MODEL

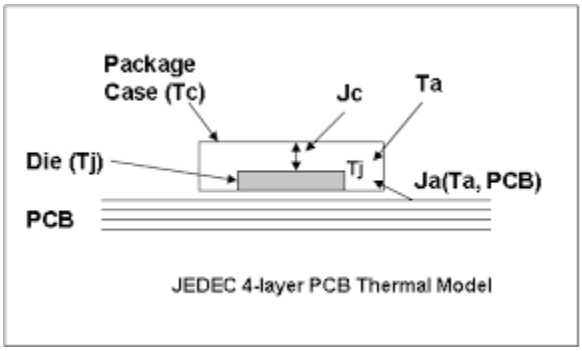


FIGURE 3 - TJ CALCULATION USING TA

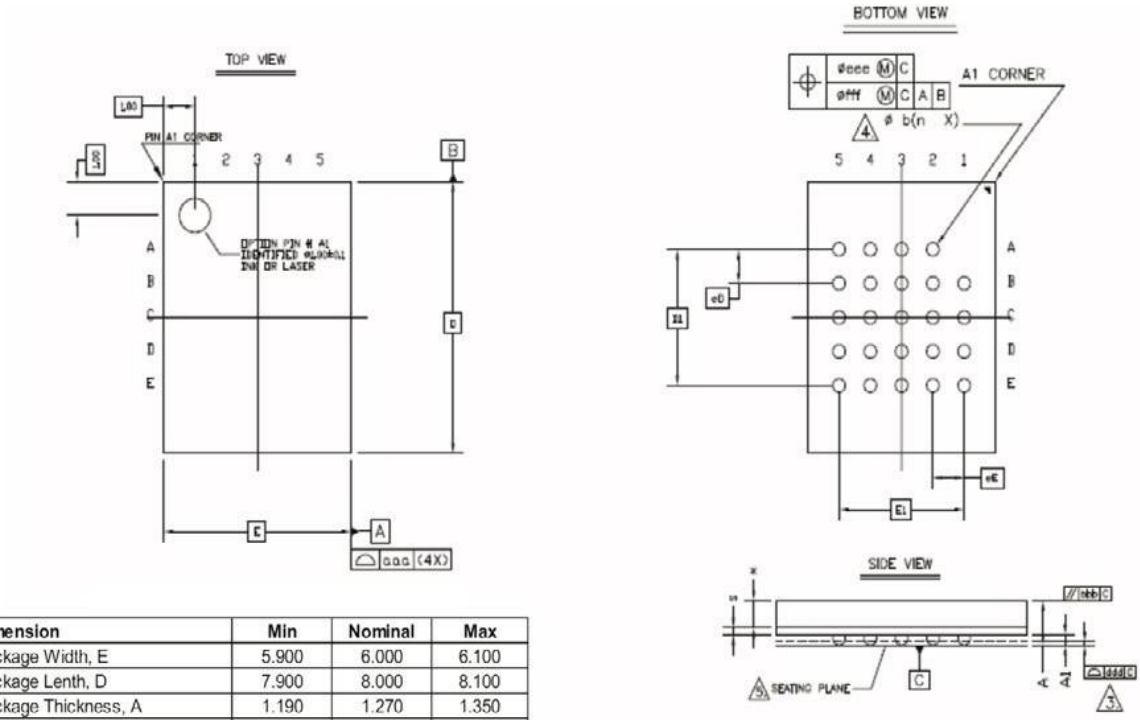
$$Tj = Ta + Rth(j\text{-}a) \times P$$

Ta : Temperature of ambient atmosphere (= room temperature where the measurement was done)
Rth(j-a) : Thermal resistance inbetween Junction and Ambient atmosphere *
P : Power dissipation **

Package Outline Drawings By Product Family

Product Family	Density and I/O Width	BGA Package Outline Drawing
MR10Q010	1Mb x8	6x8mm 24-BGA Figure 4
EMxxLX	xxx Mbit xSPI	6x8mm 24-BGA Figure 5

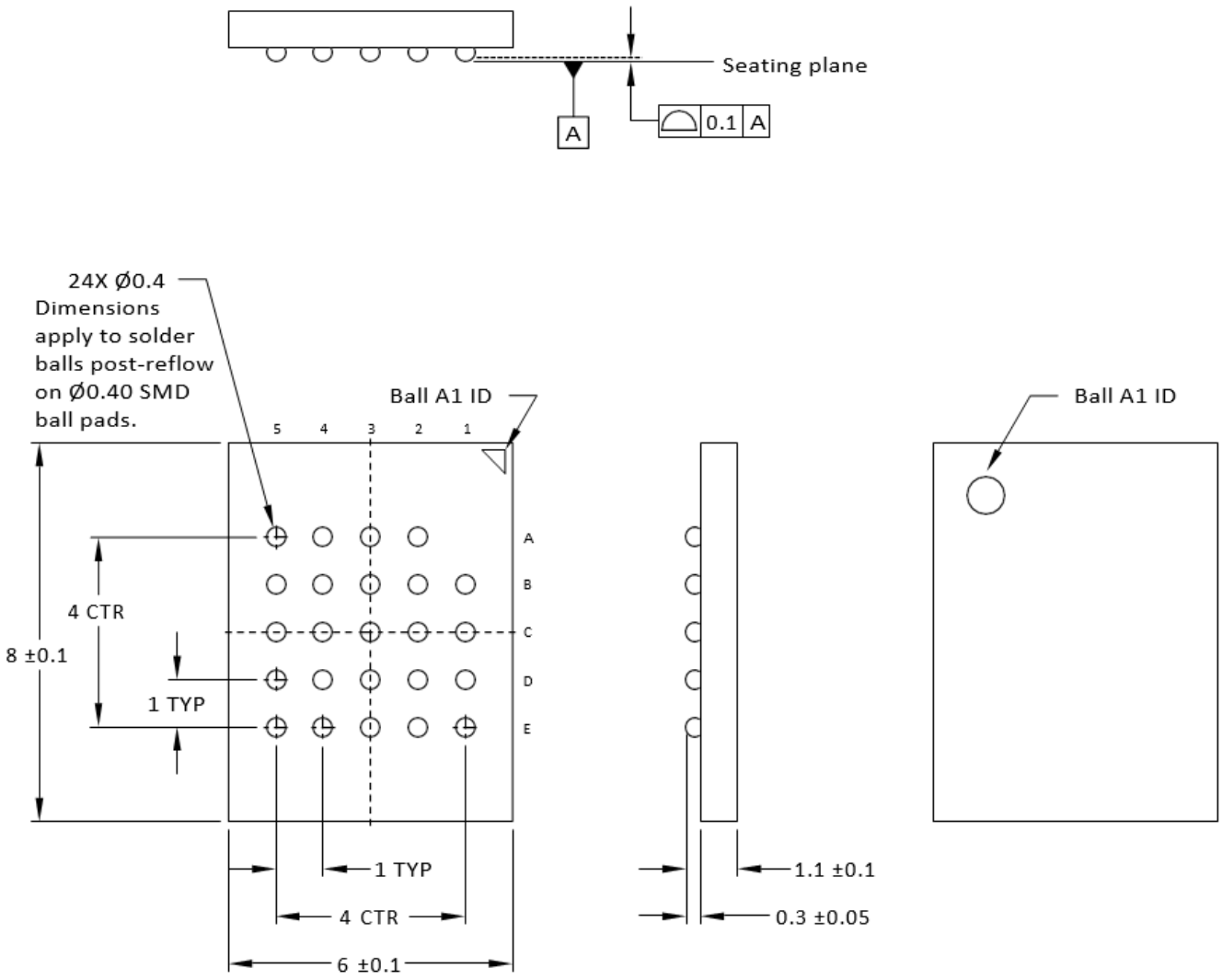
FIGURE 4 - PACKAGE OUTLINE 6X8MM 24-BALL BGA



Dimension	Min	Nominal	Max
Package Width, E	5.900	6.000	6.100
Package Lenth, D	7.900	8.000	8.100
Package Thickness, A	1.190	1.270	1.350
Solder Ball Stand-Off, A1	0.220		0.320
Solder Ball Width, b	0.320		0.420
Solder Ball Diameter		0.350	
Solder Ball Pitch, eE		1.000	
Solder ball Pitch, eD		1.000	
package Edge Tolerance, aaa		0.100	
Mold Flatness, bbb		0.200	
Solder Ball Coplanarity, ddd		0.080	
Solder Offset (Package)		0.150	
Solder Offset (Ball)		0.080	
Edge Ball Center to Center, E1		4.000	
Edge Ball Center to Center, D1		4.000	
Ball Count, n		24	

Notes:	
1	Dimensions and tolerances per ASME Y14.5M - 1994.
2	Solder ball position designation per JESD 95-1, SPP-010.
3	This dimension includes stand-off height, packge body thickness and lid height, but does not include attached features, e.g. external heatsink or chip capacitors. An intergral heatslug is not considered an attached feature.
4	Dimension is measured at the maximum solder ball diameter, parallel to primary Datum C.
5	Primary Datum C and the seating plane are defined by the spherical crowns of the solder balls.
6	All dimensions are in millimeters.

FIGURE 5 - PACKAGE OUTLINE 6X8 24-BALL TBGA



Notes: 1. All dimensions are in millimeters.

Revision History

Revision	Date	Description of Change
1.0	May 21, 2018	Initial Release
1.1	June 28, 2022	Added EMxxLX Product Family
1.2	Feb 15, 2023	Added Thermal Calculation section. Updated formatting to conform with latest Everspin format template.

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