EMxxLX as a Unified Memory Architecture

Introduction

The EMxxLX family is the latest generation of MRAM devices based on Everspin's STT (Spin-transfer Torque) technology. It is a family of high performance, multiple I/O, SPI compatible MRAM devices featuring a low pin count SPI bus interface with supported frequencies up to 200 Mhz. When the EMxxLX is configured for DTR operation with a clock speed of 200Mhz, transfer rates of 400MBps are achievable.

With the availability of larger capacity EMxxLX MRAM, 64Mb and 128Mb, it is possible to utilize one device in systems that previously utilized up to three different memory types.

For example, in some IOT systems the boot or configuration code is stored in NOR Flash, NV RAM is used for data logging and Embedded NAND for data storage. With the non-volatile nature of EMxxLX and the high-speed Reads and Writes, one device can accomplish all three tasks.

Contents

Unified Memory Overview

A Unified Memory Architecture is defined as having one memory device to meet the needs of what was previously accomplished by two or three separate memory devices.

For example, Figure 1 depicts a generic or typical IOT device utilizing NOR Flash memory for boot code or FW configuration files. A separate NV RAM is utilized for Data logging and an Embedded NAND module is used for data storage. Depending on total capacity needs, one EMxxLX device can support all three workloads.

With the advent or addition of larger capacity Everspin MRAM devices with very high-speed Read and Write capabilities, it is now possible to have one device fulfill all the requirements previously allocated to three separate devices. When utilizing one MRAM device, using the proper configurations and commands can help simplify and optimize device usage. Subsequent sections of this application note will outline the specific device settings and command optimizations.

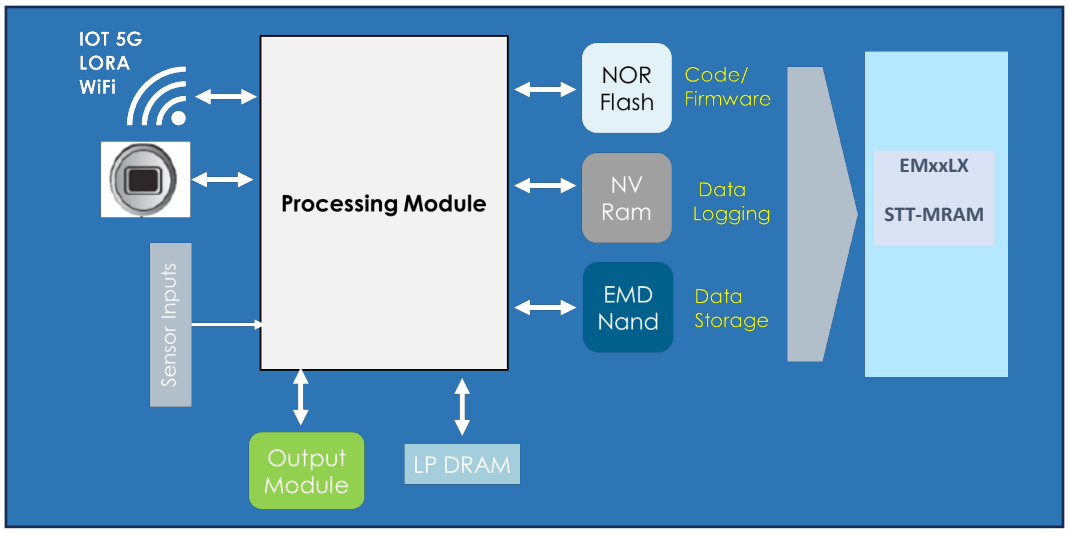

FIGURE 1 EMXXLX AS UNIFIED NON-VOLATILE MEMORY SUPPORTING HIGH SPEED READ/WRITES

Using EMxxLX for Boot code or configuration

When using the EMxxLX as media for Boot or Configuration code, certain device settings will help ensure the integrity of boot code area.

Over writing the boot code or configuration code can have detrimental effects on system initialization and configuration. To avoid this scenario, it is possible to implement protected memory areas or Block Protection schemes. Through EMxxLX device configuration settings, it is possible to protect the boot code or configuration area from inadvertent overwrites or erases.

The next section Block Protection Schemes provides details on device configuration specifics.

Block Protection Schemes

EMxxLX family of devices supports device configuration settings allowing the user to protect specific memory areas known as Block Protection. These settings allow the user to protect defined areas of the memory array. Depending upon system architecture these protected areas can be set to the top or bottom of the memory array.

Block protection allows for protection of device boot or configuration code from inadvertent erasing or overwriting. This will ensure system stability and operation.

Block protection schemes are controlled by Block Protect BP[3:0] bits and Top/Bottom bit located in the EMxxLX status register. The various settings of the TB bit and BP bits determine which sectors or segments of the array are protected.

Refer to section 5.2 Hardware Write Protection of EMxxLX/LXB data sheets for details on Block Protection schemes.

Write Streaming

When writing data in large streams or blocks, EMxxLX has features that allows for reduction in firmware overhead. Depending on device configuration, either SPI, Quad SPI, or Octal SPI, the proper write command must be selected.

For example, if EMxxLX is configured for Octal SPI with DTR, Write FAST Octal Input command (82h) would be used. If the memory device is of a larger density requiring 4 byte addressing, Write FAST Octal Input Extended (C2h) would be used.

The use of Write Fast commands allows input of one address command and multiple data with zero additional command intervention. The amount of data written can be one byte up to the full array capacity if required.

For additional details on Read and Write operation please Refer to section 10 of EMxxLX/LXB data sheets.

EMxxLX and Data logging

Many Embedded and IOT systems require storage of critical system and device operational parameters. This is commonly referred to as data logging. The ability to store this sensitive data in an efficient manner is crucial for proper analysis and targeted response by the system.

With byte addressability and sub 80ns access times for Read and Write operations, the EMxxLX performs data logging extremely efficiently, as frequently as required for the life of the sytem. Unlimited endurance over the life the product make device wear out considerations an item of minimal consideration.

EMxxLX for Data Storage

With the ability to retain user or system data for 10 years or more at high temperature, EMxxLX devices are excellent for data storage.

Many current systems have critical system data that must be stored over a long period of time. This data must be retrievable at any instant and guaranteed accurate. With EMxxLX data protection schemes, critical mission or system data will be available when as needed.

Conclusion

One EMxxLX products can fulfill the requirements that previously required up to 3 separate memories. Using one device simplifies system hardware architecture, firmware, and lowers cost.

Everspin's Industrial STT-MRAM with extremely fast Read/Write capabilities, byte address ability, unlimited endurance over the life of the device, and 10 year data retention make it an excellent solution to simplify and unify memory architecture in embedded systems.

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