Introduction

The EMxxLX family is the latest generation of MRAM devices based on Everspin's STT (Spin-transfer Torque) technology. It is a high performance, multiple I/O, SPI compatible MRAM device featuring a low pin count SPI bus interface with supported frequencies up to 200 Mhz. When the EMxxLX is configured for DTR operation with a clock speed of 200Mhz, transfer rates of 400MBps are achievable.

EMxxLX is designed as a 1.8V core and I/O signaling level device. If EMxxLX is being designed into systems without native 1.8V signaling, voltage level translation or Level Shifting is required.

A level shifter will take EMxxLX 1.8V I/0 and shift it to the required Host controller I/0 voltage. When designing in a level shifter certain considerations, such as providing appropriate voltages and level shifter timing impact must be accounted for.

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Level Shifter Voltage and Power Considerations

When implementing a level shifter, the appropriate voltages for the Level Shifter and EMxxLX device must be considered.

A typical use case using EMxxLX 1.8V I/O in a 3.3V IO system will be examined. In this case the Level shifter will be Shifting the Master Device 3.3V I/0 to Slave EMxxLX 1.8V I/O.

There are multiple level shifters from many different manufactures. The level shifter selection process is left to the system designer and beyond the scope of this document.

For example purposes, the Texas Instruments SN74ACV24T245 and LSF0102 were selected. Level shifting capabilities are rated from 1.2V-3.6V with maximum data rate of 380Mbs (1.8V to 3.3V Translation).

For proper level shifter functionality, it must be sourced with both 1.8V and 3.3V. It is assumed the Master controller requires 3.3V for I/O and has a 3.3V voltage plane. If possible, the source of 3.3V plane could be used to source the 3.3V requirements of the level shifter. If the platform has a 1.8V plane this may be used to source the 1.8V requirements of the level shifter.

Careful consideration must be used when using existing power sources to power the level shifter. The power requirements of the level shifter must not exceed the sourcing capabilities of the platforms power delivery network.

Level Shifter Timing Considerations

All Level shifters have an inherent Propagation Delay (Pd) associated with the device. This delay is the time required to switch and level shift the input signal to the output. The propagation delay must be accounted for when selecting the appropriate level shifter.

As a rule of thumb, the smaller the propagation delay the better. The timing parameters to consider when selecting a level shifter are:

A) Frequency or Clock Period of Master Controller
B) Propagation delay of level shifter
C) Set up and Hold time requirements of the Master and Slave.

For example, if the xSPI, QSPI or SPI bus is operating at 100Mhz the clock period is 10ns. If operating in DTR mode the period is 5ns, as data will be transferred on both the rising and falling edge of the clock or DS (Data Strobe) if supported.

When determining the impact of the Level Shifter propagation delay, subtract the level shifter propagation delay from the system timing window.

Level Shifter Directional Control

Depending upon the level shifter selection/implementation, directional Control may or may not be required. Direction control is defined as the direction of data flow, either to or from the EMxxLX device.

If direction control is required, a dedicated logic pin on the Master controller is used to control the direction of data during Reads/Writes to the EMxxLX device.

If direction control pin is not available, follow the level shifter manufactures design guidelines for the proper implementation and connection scheme.

Typical Level Shifter Implementations

For illustrative purposes Figure 1 and Figure 2 depict two typical level shifter implementations using the TI LSF0102 and SN74AVC24T245. The depictions below are for example purposes only and may not depict the designer's specific implementation. Follow the manufactures recommended design guidelines to ensure the level shifter implementation meets the design criteria.

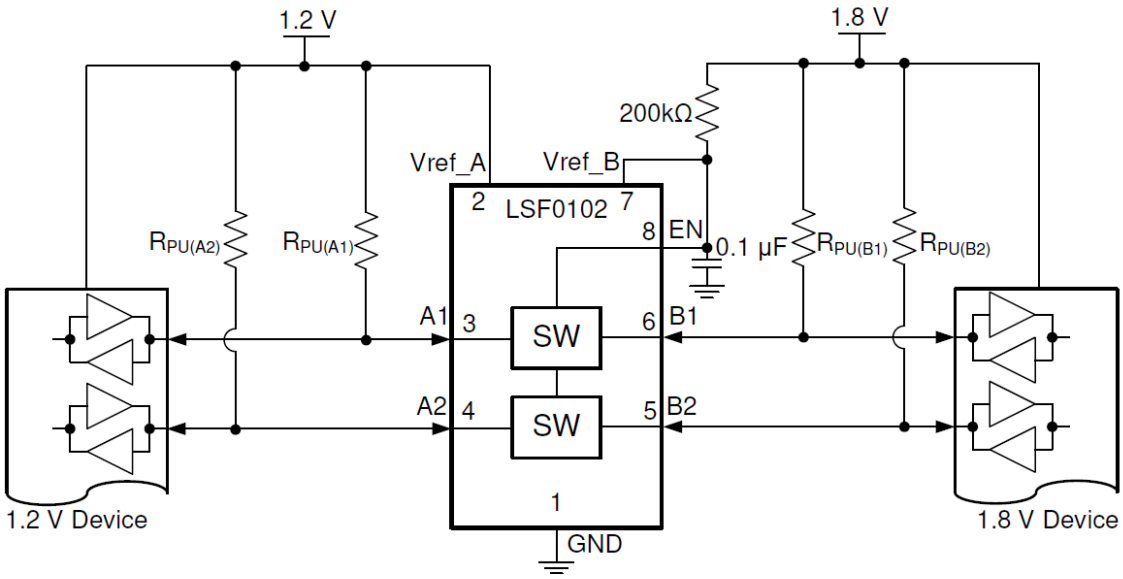

FIGURE 1 EXAMPLE LSF0102 LEVEL SHIFTER IMPLEMENTATION AUTOMATIC DIRECTION CONTROL

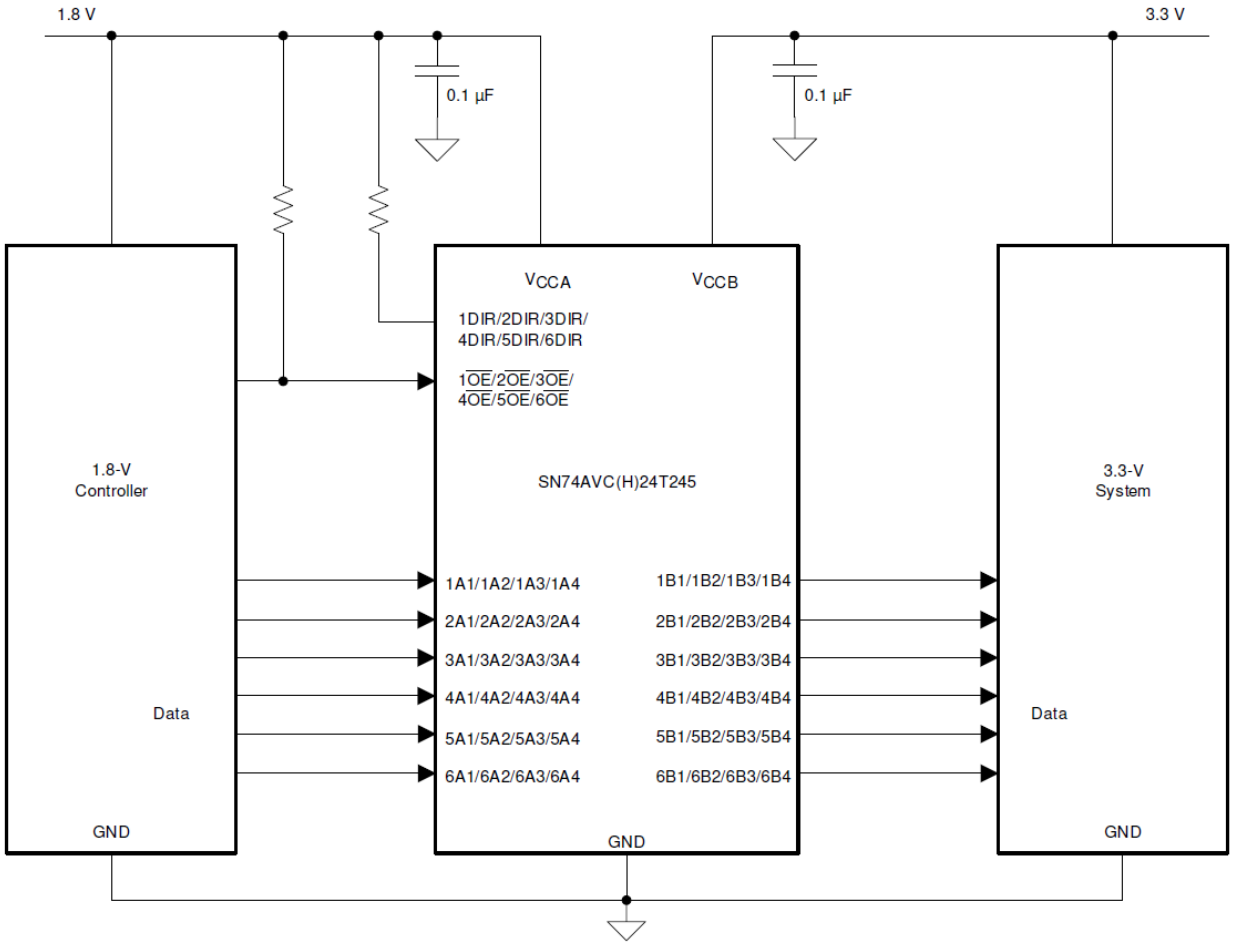

FIGURE 2 EXAMPLE SN74AVC24T245 LEVEL SHIFTER IMPLEMENTATION WITH DIRECTION CONTROL

Conclusion

In certain designs where the Master controller's IO voltage is not 1.8V, a level shifter may be designed in to translate or shift the 1.8V to the desired logic level. Care must be taken to ensure proper voltages and timing impact of the level shifter are understood and accommodated for.

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