Introduction

EMxxLX is the latest generation of MRAM devices based on Everspin's STT (Spin-Transfer Torque) technology. It is a high-performance, multiple I/O SPI compatible MRAM device featuring a low pin count SPI bus interface with supported frequencies up to 200 Mhz. When EMxxLX is configured for DTR operation with a clock speed of 200Mhz, transfer rates of 400MBps are achievable.

When using the EMxxLX in NOR emulation mode device settings and command usage can be optimized for device performance. This application note will outline the required device setup and command usage. Please reference the full EMxxLX data sheet, as it is referenced thought this application note.

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Device Settings for NOR Emulation Mode

For proper NOR emulation mode of operation the EMxxLX must be configured correctly. This mode is controlled by Nonvolatile and Volatile configuration register settings. Specifically, Nonvolatile and Volatile Configuration register 8, Bit 0.

When NOR emulation mode is desired after power on, the user will program the Nonvolatile Configuration Register. If the desired mode of operation switching in/out of NOR emulation mode during run time, Volatile Register settings should be used. Both register descriptions are included below in Figure 1 and Figure 2.

Nonvolatile Configuration Register 8					
Address	**0x0008**				
Bit	**Op**	**Name**	**Settings**	**Description**	**Notes**
7	RW	Erase Bit Value	1 = Erase with '1' (default) 0 = Erase with '0'	Determines data state for Erase operations	
6:3	RW	TBD	TBD		
3	RW	OTP Unlock			
1	RW	RPE	1 = Reset Pin Disabled (default) 0 = Reset Pin Enabled	When the Reset pin is disabled, the RESET # will be ignored. The device may be reset with Soft Reset or JESD Reset. In the DFN package option, the RESET# signal is disabled automatically when the device is configured in Quad SPI mode (Register 0).	
0	RW	Write mode	1 = Persistent Memory Mode enabled (default) 0 = Persistent memory mode disabled	Persistent Memory mode or NOR Flash like mode is selected with this bit.	4

FIGURE 1 NONVOLATILE CONFIGURATION REGISTER 8

Volatile Configuration Register 8					
Address	**0x0008**				
Bit	**Op**	**Name**	**Settings**	**Description**	**Notes**
7	RW	Erase Bit Value	1 = Erase with '1' (default) 0 = Erase with '0'	Determines data state for Erase operations	
6:2	RW	TBD	TBD		
1	RW	RPE	1 = Reset Pin Disabled (default) 0 = Reset Pin Enabled	When the Reset pin is disabled, the RESET # will be ignored. The device may be reset with Soft Reset or JESD Reset. In the DFN package option, the RESET# signal is disabled automatically when the device is configured in Quad SPI mode (Register 0).	
0	RW	Write mode	1 = Persistent Memory Mode enabled (default) 0 = Persistent memory mode disabled	Persistent Memory mode or NOR Flash like mode is selected with this bit.	4

FIGURE 2 VOLATILE CONFIGURATION REGISTER 8

NOR Emulation Command Usage

All Write (Program) commands can be used in when in NOR emulation mode. All available commands are defined in Write (Program) Operations section of the EMxxLX data sheet.

Address Wrap Considerations

In NOR emulation mode each write command commits a 256 Byte page to the array. The address control mechanism while in NOR emulation mode, wraps the lower 8 address bits back to 0x00h once 0xFFh is reached. The upper address bits remain unchanged.

It is important to note if the memory write payload is > 256 Bytes, segment the desired payload into 256 Byte increments. For example, a 4Kbyte payload would be segmented into 16 individual 256 Byte Writes.

Payload Size/256 Bytes = Number of Segments

In NOR emulation mode keep write data size <= 256 Bytes to avoid address wrap overwrite conditions.

XIP (Execute-in-Place) Configuration Settings

When in XIP (Execute-in-Place) mode, this configuration allows memory to be read by sending one address to the device without a command code and then receive the data on one, two, four or eight pins in parallel, depending on the configuration. XIP mode saves instruction overhead and reduces random access time.

EMxxLX supports XIP mode of operation when properly configured. XIP allow designers the flexibility to store code externally and not on die locally. This flexibility allows for larger external storage without impacting die size.

For additional detailed information on the EMxxLX XIP settings and configuration methodology refer to section 12, XIP (Execute-in-Place) Mode in the EMxxLX data sheet.

NOR Emulation vs Persistent Memory Considerations

Several factors should be considered when determining the desired mode of operation.

Persistent Mode of operation:

1) Byte accessibility: Data can be written to any array address on byte level granularity.
2) Variable payload: Writes size can vary from 1 Byte to Full Array.
3) Random Access: Data can be written to any address at any time.

NOR Emulation Mode of Operation:

1) 256 Byte Page write for each write command
2) Maintain SW compatibility with previous code base
    a. Previous payload size of code base should be accounted for. If previous code used 4Kbyte page writes, please refer to Address Wrap considerations section.

Conclusion

Everspin's latest generation of STT MRAM device the EMxxLX offers design flexibility and speed with it latest xSPI implementation. EMxxLX offers users the flexibility of multiple configurations. The device can be configured in NOR emulation, Persistent Memory and XIP modes of operation supporting multiple usage models with minimal code modification or changes from previous NOR architectures.

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