United States (US) Patent Marking for Everspin STT-MRAM 256Mb products are identified below. The patents apply to all configurations and skus, unless stated differently. The products may be sold individually or as part of a solution. If you have any questions about this list, please contact our Patent Counsel: Dinesh Melwani - dmelwani@bomcip.com; 202.808.3497.

STT-MRAM Product Family covered by these patents include:
EMD4E001G

Patents listed in numerical order:

Patent #	Patent Title
6205052	MAGNETIC ELEMENT WITH IMPROVED FIELD RESPONSE AND FABRICATING METHOD THEREOF
6549454	TMR MATERIAL HAVING A SUBSTANTIALLY SMOOTH AND CONTINUOUS ULTRA-THIN MAGNETIC LAYER
6760266	SENSE AMPLIFIER AND METHOD FOR PERFORMING A READ OPERATION IN A MRAM
6784510	MAGNETORESISTIVE RANDOM ACCESS MEMORY DEVICE STRUCTURES AND METHODS FOR FABRICATING THE SAME
6881351	METHODS FOR CONTACTING CONDUCTING LAYERS OVERLYING MAGNETOELECTRONIC ELEMENTS OF MRAM DEVICES
6890770	MAGNETORESISTIVE RANDOM ACCESS MEMORY DEVICE STRUCTURES AND METHODS FOR FABRICATING THE SAME
6911156	METHODS FOR FABRICATING MRAM DEVICE STRUCTURES
7031183	MRAM DEVICE INTEGRATED WITH OTHER TYPES OF CIRCUITRY
7098495	MAGNETIC TUNNEL JUNCTION ELEMENT STRUCTURES AND METHODS FOR FABRICATING THE SAME
7224630	ANTIFUSE CIRCUIT
7370260	MRAM HAVING ERROR CORRECTION CODE CIRCUITRY AND METHOD THEREFOR
7476329	METHODS FOR CONTACTING CONDUCTING LAYERS OVERLYING MAGNETOELECTRONIC ELEMENTS OF MRAM DEVICES
7532533	ANTIFUSE CIRCUIT AND METHOD FOR SELECTIVELY PROGRAMMING THEREOF
7605437	SPIN-TRANSFER MRAM STRUCTURE AND METHODS
8119424	ELECTRONIC DEVICE INCLUDING A MAGNETO-RESISTIVE MEMORY DEVICE AND A PROCESS FOR FORMING THE ELECTRONIC DEVICE
8216703	MAGNETIC TUNNEL JUNCTION DEVICE
8236578	ELECTRONIC DEVICE INCLUDING A MAGNETO-RESISTIVE MEMORY DEVICE AND A PROCESS FOR FORMING THE ELECTRONIC DEVICE
8355272	MEMORY ARRAY HAVING LOCAL SOURCE LINES
8497538	MRAM SYNTHETIC ANTIFERROMAGNET STRUCTURE
8685756	METHOD FOR MANUFACTURING AND MAGNETIC DEVICES HAVING DOUBLE TUNNEL BARRIERS

Patent #	Patent Title
8686484	SPIN-TORQUE MAGNETORESISTIVE MEMORY ELEMENT AND METHOD OF FABRICATING SAME
8747680	METHOD OF MANUFACTURING A MAGNETORESISTIVE-BASED DEVICE
8754460	MRAM SYNTHETIC ANITFEROMAGNET STRUCTURE
8790935	A METHOD OF MANUFACTURING A MAGNETORESISTIVE-BASED DEVICE WITH VIA INTEGRATION
8811071	METHOD OF WRITING TO A SPIN TORQUE MAGNETIC RANDOM ACCESS MEMORY
8817530	DATA-MASKED ANALOG AND DIGITAL READ FOR RESISTIVE MEMORIES
8877522	METHOD OF MANUFACTURING A MAGNETORESISTIVE-BASED DEVICE WITH VIA INTEGRATION
8923041	SELF-REFERENCED SENSE AMPLIFIER FOR SPIN TORQUE MRAM
8929132	WRITE DRIVER CIRCUIT AND METHOD FOR WRITING TO A SPIN-TORQUE MRAM
8976610	MEMORY DEVICE WITH TIMING OVERLAP MODE
8984379	MRAM FIELD DISTURB DETECTION AND RECOVERY
9007811	WORD LINE DRIVER CIRCUIT
9019794	MEMORY DEVICE WITH REDUCED ON-CHIP NOISE
9047965	CIRCUIT AND METHOD FOR SPIN-TORQUE MRAM BIT LINE AND SOURCE LINE VOLTAGE REGULATION
9047967	DATA-MASKED ANALOG AND DIGITAL READ FOR RESISTIVE MEMORIES
9047969	METHOD OF WRITING TO A SPIN TORQUE MAGNETIC RANDOM ACCESS MEMORY
9054297	MAGNETIC RANDOM ACCESS MEMORY INTEGRATION HAVING IMPROVED SCALING
9093637	MRAM SYNTHETIC ANITFEROMAGNET STRUCTURE
9093640	METHOD FOR MANUFACTURING AND MAGNETIC DEVICES HAVING DOUBLE TUNNEL BARRIERS
9111622	SELF REFERENCING SENSE AMPLIFIER FOR SPIN TORQUE MRAM
9112536	METHOD OF READING AND WRITING TO A SPIN TORQUE MAGNETIC RANDOM ACCESS MEMORY WITH ERROR CORRECTING CODE
9136464	APPARATUS AND PROCESS FOR MANUFACTURING ST-MRAM HAVING METAL OXIDE TUNNEL BARRIER
9159906	SPIN-TORQUE MAGNETORESISTIVE MEMORY ELEMENT AND METHOD OF FABRICATING SAME
9166155	METHOD OF MANUFACTURING A MAGNETORESISTIVE-BASED DEVICE
9183912	CIRCUIT AND METHOD FOR CONTROLLING MRAM CELL BIAS VOLTAGES
9196342	CIRCUIT AND METHOD FOR SPIN-TORQUE MRAM BIT LINE AND SOURCE LINE VOLTAGE REGULATION
9218865	SELF-REFERENCED SENSE AMPLIFIER FOR SPIN TORQUE MRAM
9230632	WORD LINE DRIVER CIRCUIT
9230633	MEMORY DEVICE WITH TIMING OVERLAP MODE
9245611	METHOD OF WRITING TO A SPIN TORQUE MAGNETIC RANDOM ACCESS MEMORY
9257165	ASSISTED LOCAL SOURCE LINE
9269894	ISOLATION OF MAGNETIC LAYERS DURING ETCH IN A MAGNETORESISTIVE DEVICE

Patent #	Patent Title
9275715	NON-DESTRUCTIVE WRITE/READ LEVELING
9281168	REDUCING SWITCHING VARIATION IN MAGNETORESISTIVE DEVICES
9286218	WORD LINE AUTO-BOOTING IN A SPIN-TORQUE MAGNETIC MEMORY HAVING LOCAL SOURCE LINES
9293698	MAGNETORESISTIVE STRUCTURE HAVING A METAL OXIDE TUNNEL BARRIER AND METHOD OF MANUFACTURING SAME
9306157	METHOD OF MANUFACTURING A MAGNETORESISTIVE-BASED DEVICE
9311980	WORD LINE SUPPLY VOLTAGE GENERATOR FOR A MEMORY DEVICE AND METHOD THEREFORE
9343661	NON-REACTIVE PHOTORESIST REMOVAL AND SPACER LAYER OPTIMIZATION IN A MAGNETORESISTIVE DEVICE
9361964	BOOSTED SUPPLY VOLTAGE GENERATOR FOR A MEMORY DEVICE AND METHOD THEREFORE
9368181	CIRCUIT AND METHOD FOR ACCESSING A BIT CELL IN A SPIN-TORQUE MRAM
9378796	METHOD FOR WRITING TO A MAGNETIC TUNNEL JUNCTION DEVICE
9378798	METHOD OF WRITING TO A SPIN TORQUE MAGNETIC RANDOM ACCESS MEMORY
9391264	MAGNETORESTIVE MTJ STACK HAVING AN UNPINNED, FIXED SYNTHETIC ANTI-FERROMAGNETIC STRUCTURE
9401195	SELF-REFERENCED SENSE AMPLIFIER FOR SPIN TORQUE MRAM
9419208	MAGNETORESISTIVE MEMORY ELEMENT AND METHOD OF FABRICATING SAME
9431602	TOP ELECTRODE COUPLING IN A MAGNETORESISTIVE DEVICE USING AN ETCH STOP LAYER
9444037	MAGNETERESISTIVE MEMORY ELEMENT HAVING A METAL OXIDE TUNNEL BARRIER
9454432	METHOD OF READING AND WRITING TO A SPIN TORQUE MAGNETIC RANDOM ACCESS MEMORY WITH ERROR CORRECTING CODE
9502089	SHORT DETECTION AND INVERSION
9502093	METHOD OF WRITING TO A SPIN TORQUE MAGNETIC RANDOM ACCESS MEMORY
9507662	EXPANDED ERROR CORRECTION CODES
9529672	ECC WORD CONFIGURATION FOR SYSTEM-LEVEL ECC COMPATIBILITY
9529726	MEMORY DEVICE WITH PAGE EMULATION MODE
9542989	CIRCUIT AND METHOD FOR CONTROLLING MRAM CELL BIAS VOLTAGES
9543041	CONFIGURATION AND TESTING FOR MAGNETORESISTIVE MEMORY TO ENSURE LONG TERM CONTINUOUS OPERATION
9548098	NON-DESTRUCTIVE WRITE/READ LEVELING
9548442	MAGNETORESISTIVE STRUCTURE HAVING TWO DIELECTRIC LAYERS, AND METHOD OF MANUFACTURING SAME
9552849	MEMORY DEVICE WITH TIMING OVERLAP MODE AND PRECHARGE TIMING CIRCUIT
9553258	MAGNETORESISTIVE MEMORY ELEMENT AND METHOD OF FABRICATING SAME
9553260	METHOD OF INTEGRATION OF A MAGNETORESISTIVE STRUCTURE
9575125	MEMORY DEVICE WITH REDUCED TEST TIME
9583169	BOOSTED SUPPLY VOLTAGE GENERATOR AND METHOD THEREFORE

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9595665	NON-REACTIVE PHOTORESIST REMOVAL AND SPACER LAYER OPTIMIZATION IN A MAGNETORESISTIVE DEVICE
9601175	WORD LINE AUTO-BOOTING IN A SPIN-TORQUE MAGNETIC MEMORY HAVING LOCAL SOURCE LINES
9691442	MEMORY DEVICE WITH REDUCED ON-CHIP NOISE
9697880	SELF-REFERENCED READ WITH OFFSET CURRENT IN A MEMORY
9698341	MAGNETORESISTIVE DEVICE AND METHOD OF MANUFACTURING SAME
9722176	ISOLATION OF MAGNETIC LAYERS DURING ETCH IN A MAGNETORESISTIVE DEVICE
9728583	TOP ELECTRODE COUPLING IN A MAGNETORESISTIVE DEVICE USING AN ETCH STOP LAYER
9734884	METHOD FOR WRITING TO A MAGNETIC TUNNEL JUNCTION DEVICE
9793468	MAGNETORESISTIVE MTJ STACK HAVING AN UNPINNED, FIXED SYNTHETIC ANTI-FERROMAGNETIC STRUCTURE
9793470	MAGNETORESISTIVE STACK/STRUCTURE AND METHOD OF MANUFACTURING SAME
9837603	POST-ETCH ENCAPSULATION FOR A MAGNETORESTIVE DEVICE
9847116	CIRCUIT AND METHOD FOR CONTROLLING MRAM CELL BIAS VOLTAGES
9865804	MAGNETORESISTIVE DEVICE AND METHOD OF MANUFACTURING SAME
9870812	MEMORY SYSTEM WITH TIMING OVERLAP MODE FOR ACTIVATE AND PRECHARGE OPERATIONS
9881695	SHORT DETECTION AND INVERSION
9893275	MAGNETORESISTIVE STRUCTURE HAVING TWO DIELECTRIC LAYERS, AND METHOD OF MANUFACTURING SAME
9911481	SELECTION CIRCUIT WITH AUTOBOOTING FOR MAGNETIC MEMORY AND METHODS THEREFORE
9947865	MAGNETORESISTIVE STACK AND METHOD OF FABRICATING SAME
9972373	SELF-REFERENCED READ WITH OFFSET CURRENT IN A MEMORY
9978433	NON-DESTRUCTIVE WRITE/READ LEVELING
9990300	DELAYED WRITE-BACK IN MEMORY
9997239	WORD LINE OVERDRIVE IN MEMORY AND METHOD THEREFOR
10020041	SELF-REFERENCED SENSE AMPLIFIER WITH PRECHARGE
10037790	WORD LINE AUTO-BOOTING IN A SPIN-TORQUE MAGNETIC MEMORY HAVING LOCAL SOURCE LINES
10056544	ISOLATION OF MAGNETIC LAYERS DURING ETCH IN A MAGNETORESISTIVE DEVICE
10056909	SINGLE-LOCK DELAY LOCKED LOOP WITH CYCLE COUNTER AND METHOD THEREFORE
10062839	MAGNETORESISTIVE DEVICE AND METHOD OF MANUFACTURING SAME
10079339	MAGNETORESISTIVE STACK/STRUCTURE AND METHOD OF MANUFACTURING SAME
10114700	MEMORY DEVICE WITH PAGE EMULATION MODE
10141498	MAGNETORESISTIVE STACK, SEED REGION THEREFOR AND METHOD OF MANUFACTURING SAME
10146601	METHOD FOR HEALING RESET ERRORS IN A MAGNETIC MEMORY
10164176	METHOD OF INTEGRATION OF A MAGNETORESISTIVE STRUCTURE

Patent #	Patent Title
10199122	SHORT DETECTION AND INVERSION
10199571	METHODS OF MANUFACTURING OF MAGNETORESISTIVE MTJ STACKS HAVING AN UNPINNED, FIXED SYNTHETIC ANTI-FERROMAGNETIC STRUCTURE
10199574	MAGNETORESISTIVE STACK AND METHOD OF FABRICATING SAME
10230046	MAGNETORESISTIVE STRUCTURE HAVING TWO DIELECTRIC LAYERS, AND METHOD OF MANUFACTURING SAME
10249364	WORD LINE OVERDRIVE IN MEMORY AND METHOD THEREFOR
10250265	SINGLE-LOCK DELAY LOCKED LOOP WITH CYCLE COUNTER AND METHOD THEREFOR
10256840	ECC WORD CONFIGURATION FOR SYSTEM-LEVEL ECC COMPATIBILITY
10262713	BIAS CONFIGURATION FOR WRITE OPERATIONS IN MEMORY
10268591	DELAYED WRITE-BACK IN MEMORY
10297747	APPARATUS AND METHODS FOR INTEGRATING MAGNETORESISTIVE DEVICES
10304511	DUAL-EDGE TRIGGER ASYNCHRONOUS CLOCK GENERATION AND RELATED METHODS
10347828	MAGNETORESISTIVE STACK AND METHOD OF FABRICATING SAME
10395699	MEMORY DEVICE WITH SHARED AMPLIFIER CIRCUITRY
10396279	MAGNETORESISTIVE DEVICE AND METHOD OF MANUFACTURING SAME
10446213	BITLINE CONTROL IN DIFFERENTIAL MAGNETIC MEMORY
10461250	MAGNETORESISTIVE STACK/STRUCTURE AND METHOD OF MANUFACTURING SAME
10461251	METHOD OF MANUFACTURING INTEGRATED CIRCUIT USING ENCAPSULATION DURING AN ETCH PROCESS
10475497	SELF-REFERENCED SENSE AMPLIFIER WITH PRECHARGE
10483320	MAGNETORESISTIVE STACK WITH SEED REGION AND METHOD OF MANUFACTURING THE SAME
10483460	METHOD OF MANUFACTURING A MAGNETORESISTIVE STACK/ STRUCTURE USING PLURALITY OF ENCAPSULATION LAYERS
10516103	MAGNETORESISTIVE STACK AND METHOD OF FABRICATING SAME
10535390	MAGNETORESISTIVE DEVICES AND METHODS THEREFOR
10541362	APPARATUS AND METHODS FOR INTEGRATING MAGNETORESISTIVE DEVICES
10573365	CIRCUIT FOR WORDLINE AUTOBOOTING IN MEMORY AND METHOD THEREFOR
10608172	MAGNETORESISTIVE STRUCTURE HAVING TWO DIELECTRIC LAYERS, AND METHOD OF MANUFACTURING SAME
10608648	SINGLE-LOCK DELAY LOCKED LOOP WITH CYCLE COUNTER AND METHOD THEREFOR
10608671	ECC WORD CONFIGURATION FOR SYSTEM-LEVEL ECC COMPATIBILITY
10614907	SHORT DETECTION AND INVERSION
10622554	MAGNETORESISTIVE STACK AND METHOD OF FABRICATING SAME
10650899	DELAYED WRITE-BACK IN MEMORY WITH CALIBRATION SUPPORT
10657065	DELAYED WRITE-BACK IN MEMORY
10658013	FEED FORWARD BIAS SYSYTEM FOR MTJ VOLTAGE CONTROL
10658576	MAGNETORESISTIVE STACK/STRUCTURE AND METHOD OF MANUFACTURING SAME
10692926	MAGNETORESISTIVE STACK WITH SEED REGION AND METHOD OF MANUFACTURING THE SAME

Patent #	Patent Title
10707410	MAGNETORESISTIVE STACKS WITH AN UNPINNED, FIXED SYNTHETIC ANTI-FERROMAGNETIC STRUCTURE AND METHODS OF MANUFACTURING THEREOF
10777738	METHOD OF MANUFACTURING INTEGRATED CIRCUIT USING ENCAPSULATION DURING AN ETCH PROCESS
10847715	MAGNETORESISTIVE DEVICE AND METHOD OF MANUFACTURING SAME
10897008	MAGNETORESISTIVE STACKS WITH AN UNPINNED, FIXED SYNTHETIC ANTI-FERROMAGNETIC STRUCTURE AND METHODS OF MANUFACTURING THEREOF
10910434	MAGNETORESISTIVE STACK WITH SEED REGION AND METHOD OF MANUFACTURING THE SAME
10923170	DETERMINING BIAS CONFIGURATION FOR WRITE OPERATIONS IN MEMORY TO IMPROVE DEVICE PERFORMANCE DURING NORMAL OPERATION AS WELL AS TO IMPROVE THE EFFECTIVENESS OF TESTING ROUTINES