

Replacing the Fujitsu MB85R4M2TFN FRAM with Everspin's MR2A16ACYS35 MRAM

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EVERSPIN TECHNOLOGIES NON-VOLATILE MEMORY

Everspin Technologies is the global leader in MRAM technology. Our award-winning Toggle MRAM product family is in high volume production. The MR2A16ACYS35 is a 4Mb member of the MRAM family organized by 256K x 16.

RELIABLE SUPPLY

Everspin is a long term, reliable manufacturer of MRAM products and is located in a high volume, automotive certified, stable fabrication facility in Chandler, Arizona.

SUMMARY

The Everspin's 4Mb MRAM MR2A16ACYS35 can operate with the Fujitsu 4Mb FRAM MB85R4M2T slower timing, but also allows the system designer to take advantage of MRAM's four times faster random access cycle time. The Everspin 4Mb MRAM MR2A16ACYS35 is available in 44-Pin TSOP2 and 48-Ball BGA packages.

BENEFITS OF MR2A16ACYS35

Upgrading to Everspin MRAM provides many benefits over Fujitsu FRAM:

- Faster Random Access Operation Times
- High Reliability and Data Retention
- Unlimited Read/Write Endurance
- No Wear-out Concern
- Competitive Pricing
- Stable Manufacturing Supply Chain
- Small Footprint BGA Package

COMMON PINS

The MR2A16ACYS35 is a 4Mb non-volatile RAM organized as 256kx16 operating from a nominal 3.3V power supply and is compatible with FRAM. Both products use standard SRAM parallel address (A0-16), byte-wide bidirectional data pins (DQ0-7) and control signals (/E, /W, /G). Each can be supported by a common timing interface and will function as random access read/write memories that retain data without external battery when power is removed. Everspin does not support the /ZZ sleep function. /ZZ may require pull-up.

Parameter	MB85R4M2TFN-G-JAE2	MR2A16ACYS35	
Package	44-Pin TSOP	44-Pin TSOP	
Size and Height	10.16 × 18.41 × 1.2 mm	10.16 × 18.41 × 1.2 mm	
Pinout / Footprint	See Figure 1 and Table 2 below		
Solder Profile	Per JEDEC J-STD-020D.1		

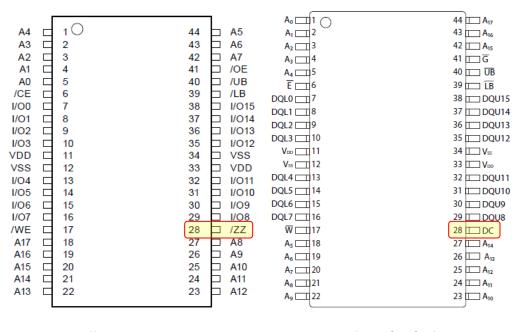
Table 1 – Overview: MB85R4M2TFN vs. MR2A16ACYS35

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Figure 1 – Pinout/Footprint Comparison and Considerations



Fujitsu

Everspin Technologies

Table	2 –	Pin	Function	Comparison
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Pin #	Fujitsu	Everspin	Everspin Definition	Everspin Comments
28	/ZZ	DC	Do Not Connect	This pin is used for test. Prefer to float. If
				driven, must be pulled to Vı∟.

MRAM PROVIDES FASTER TIMING

The MR2A16ACYS35 and MB85R4M2T use address, data, and control signals that are similar to standard SRAM. The Everspin MR2A16ACYS35, however, allows for faster read and write operations at 35ns. The Fujitsu FRAM requires a read cycle time of at least 150ns for random read accesses. The internal operation of the MB85R4M2T requires a precharge time of at least 75ns following a 75ns initial read access, resulting in a random access minimum cycle time of 150ns. The pre-charge time is present whether self-timed by the part or initiated by the user by bringing /CE high. FRAM performs the read during the initial access portion of the cycle time and then restores the data to the memory cell (writes data back) during the pre-charge time like a DRAM. This is known as destructive readout operation. MRAM can operate with this slower FRAM read sequence but MRAM is actually much faster as it does not have a destructive read mechanism. Both read and write cycles wear out the FRAM. MRAM has unlimited read and write endurance. The MR2A16ACYS35 supports a 35-ns read access and cycle time. The MR2A16ACYS35 does not require a precharge cycle and is two times faster than the FRAM on initial read access time and four times faster on random accesses. The FRAM requires 150ns to complete a write cycle just as it does a read cycle. The MRAM will operate with this timing but actually has a write cycle time of just 35 ns (4 times faster than FRAM). To take advantage of the four times faster random read and write speed of the MR2A16ACYS35, you may wish to modify the control interface. MRAM plugs directly into most SRAM controllers without change.



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POWER CYCLING CONSIDERATIONS

The MB85R4M2T has a power startup time of 450 us and a power down time of 85 ns, while the MR2A16ACYS35 is specified at 2 ms for power up and power down sequences. These differences in startup times will not be an issue in most system designs since the power-up master reset is purposely made much longer to assure that all circuitry is stabilized for start of operation.

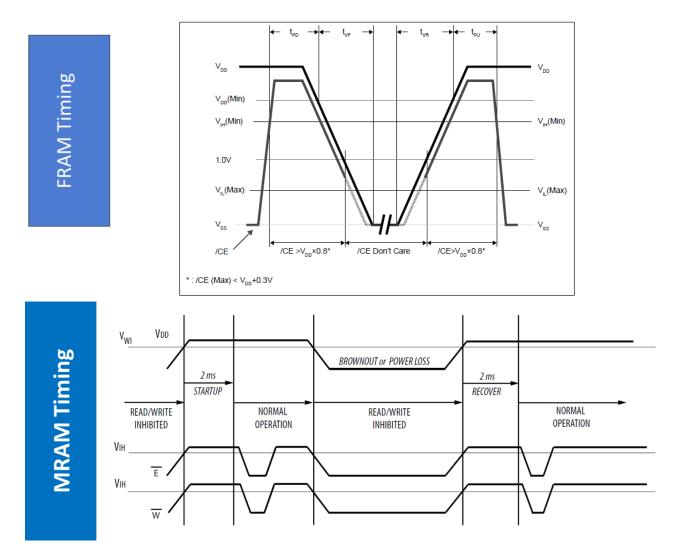


Figure 2 Power Up and Power Down Diagrams

POWER SUPPLY CONSIDERATIONS

Both the MRAM and the FRAM are specified at nominal 3.3V power supply. The FRAM has a standby current of 150 uA. To enable three times faster random access speed, MRAM's standby current is 9 mA. For battery-powered applications, designers can take advantage of MRAM's non-volatility and power gate the MRAM to reduce standby power to zero when not in use.

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READ AND WRITE CURRENTS

The read and write current for the MR2A16ACYS35 is similar than the MB85R4M2T at 20 mA active current for 150 ns cycle time. MR2A16ACYS35 is specified at max 80 mA read, 165 mA write when operating at its faster 35 ns cycle time operation.

RELIABILITY CONSIDERATIONS FOR COMPARISON

The MB85R4M2T FRAM architecture employs ferroelectric materials as storage devices. These materials have an intrinsic electric dipole switched into opposite polarities with an external electric field. A read operation in a FRAM is destructive because it requires switching the polarization state in order to sense its state. The read operation has to restore the polarization to its original state after the initial read which adds cycle time to the read operation. FRAM Read and Write cycles require an initial "Pre-charge" time which can increase the initial access time. Ambient operating temperatures above 85°C accelerate wear-out of FRAM due to build-up of free electric charge resulting in imprint.

Everspin MRAM will provide the most cost-effective non-volatile RAM solution. MR2A16ACYS35 MRAM is built using a much simpler 1-transistor, 1-magnetic tunnel junction cell. The simple Everspin MRAM cell leads to improved manufacturing efficiency and increased reliability. MRAM uses magnetic tunnel junction technology for non-volatile storage. Data does not leak away at high temperature and there is no wear-out mechanism to limit the number of read, write, or power cycles in this technology. Data retention is better than 20 years at 125°C.

SUMMARY

Replacing a MB85R4M2T with Everspin's MR2A16ACYS35 4Mb MRAM is a straight-forward process. These devices are close to a drop-in replacement with some consideration of pinout, package size and timing details shown in the application note.

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