Replacing the Cypress CY15B104QN SPI-FRAM with Everspin MR2xH40xDF SPI-MRAM

EVERSPIN MRAM MEMORY

Everspin is the worldwide leader in designing, manufacturing, and commercially shipping discrete Magnetoresistive RAM (MRAM) into markets and applications where data persistence and integrity, low latency, and security are paramount. The MR2xH40xDF is a family of 4,194,304-bit magnetoresistive random access memory (MRAM) devices organized as 524,288 words of 8 bits. They are the ideal memory solution for applications that must store and retrieve data and programs quickly using a small number of I/O pins. They have serial EEPROM and serial Flash compatible read/write timing with no write delays and unlimited read/write endurance. Unlike other serial memories, with the MR2xH40xDF family both reads and writes can occur randomly in memory with no delay between writes.

OVERVIEW

The MR2xH40xDF family is an SPI interface MRAM family with a memory array logically organized as 512Kx8 using the four pin interface of chip select (CS), serial input (SI), serial output (SO) and serial clock (SCK) of the serial peripheral interface (SPI) bus. The MRAM implements a subset of commands common to SPI EEPROM and SPI Flash components. This allows the SPI MRAM to replace these components in the same socket and interoperate on a shared SPI bus. The SPI MRAM offers superior write speed, unlimited endurance, low standby & operating power, and simple, reliable data retention compared to other serial memory alternatives.

RELIABLE SUPPLY

Everspin is a long term, reliable manufacturer of MRAM products and operates a fabrication facility in Chandler, Arizona.

BENEFITS OF MR2xH40xDF

Upgrading to Everspin MRAM provides many benefits over Cypress FRAM:

- Faster Random Access Operation Times (50MHz/20ns tCLK and 40MHz/25ns tCLK)
- High Reliability and Data Retention (greater than 20 years at 125C Operating Temperature)
- Unlimited Read/Write Endurance
- No Wear-out Concern
- Automatic Data Protection On Power Loss
- Competitive Pricing
- Stable Manufacturing Supply Chain

COMMON PINS

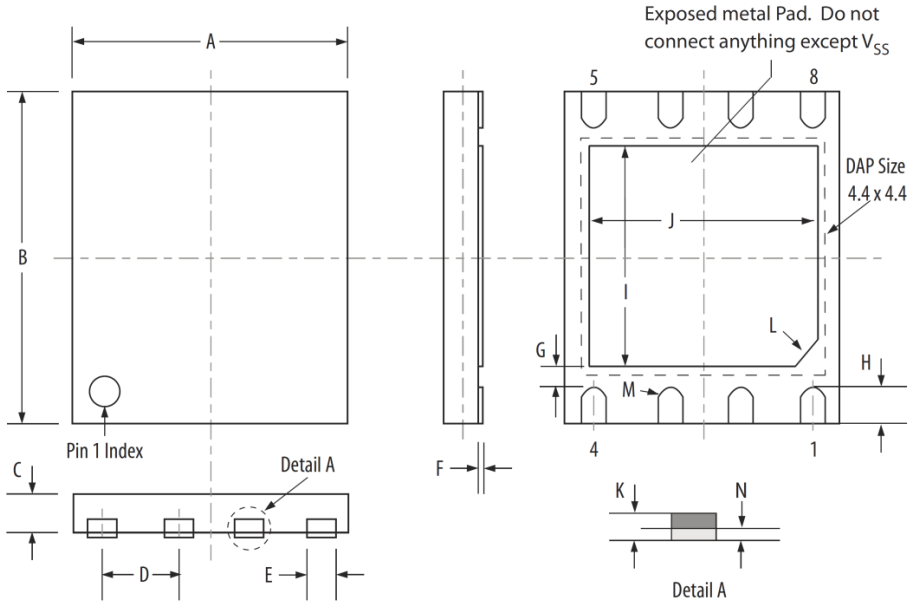
The MR2xH40xDF is a 4Mb non-volatile RAM organized 512Kx8 operating from a nominal 3.3V power supply and is compatible with FRAM. It is available in a standard 8-pin Small Flag DFN (DF version) and 8-pin DFN (DC version), which are versatile package options to make it a close replacement with SPI-FRAM 8-pin SOIC and 8-pin GQFN packages (Table 1). From a hardware point of view, the key difference is the change in the PCB for package pinout (pin 7). From a software point of view, the key difference between the two devices are pin 7 functionality, and Device ID. The HOLD# pin (pin 7) for MR2xH40xDF is used when the host CPU must interrupt a memory

operation for another task. When HOLD# is LOW, the current operation is suspended. The device ignores any transition on SCK or CS#. All transitions on HOLD# must occur while SCK is LOW. This pin must be tied to VDD if not used. A hardware and software change may be required to enable HOLD# function on the MRAM. Pin 7 on the FRAM is DNU, or do not use.

Table 1. Pin and Package Comparison

Feature/Function	SPI MRAM (MR2xH40)	SPI F-RAM (CY15B104QN)	Comments
8-pin DFN Exposed Metal PAD	Do not connect anything except VSS	Not available	The Exposed Metal Pad of the MRAM 8-pin DFN package is an NC (No Connect) pad; therefore, it can be either floating or connected to VSS. Everspin does not recommend soldering the MRAM DFN Exposed Metal Pad on the PCB
8-pin packages	8-pin DFN (MR2xH40xDC) 8-pin DFN (Small Flag) (MR2xH40xDF)	8-pin GQFN, 8-pin SOIC	Both 8-pin DFN MRAM packages as shown in Figure 1 and Figure 2 are compatible with the 8-pin SOIC package of FRAM as shown in Figure 3. Different layout consideration is needed when replacing the 8-pin GQFN FRAM package (Figure 4)
Pin 7 function	HOLD#	DNU	See HOLD# function in MR2xH40 datasheet.

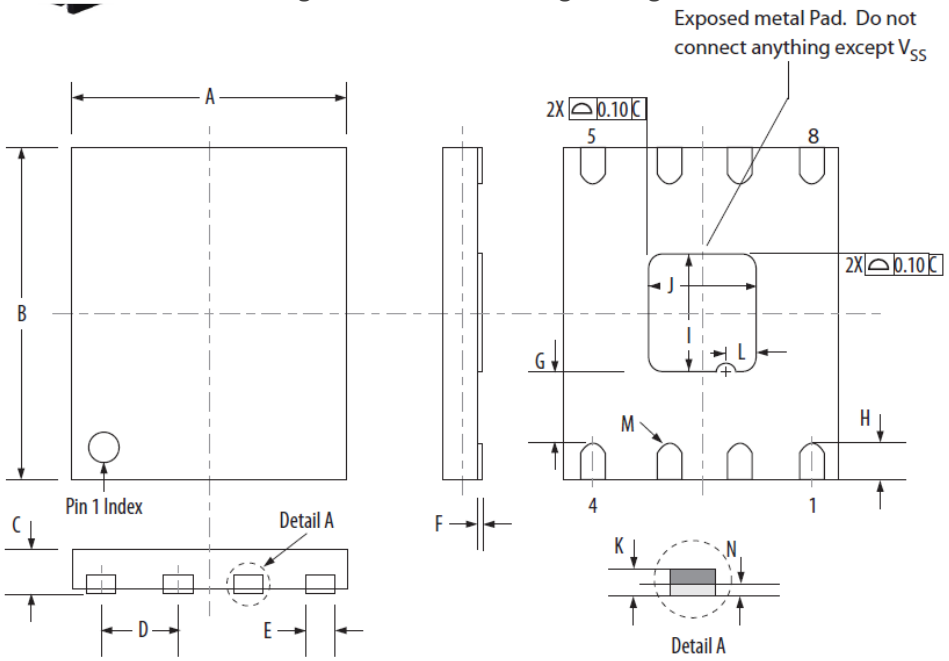
Figure 1 - Mbit SPI MRAM 8-pin DFN Package Outline



Dimension	A	B	C	D	E	F	G	H	I	J	K	L	M	N
Max.	5.10	6.10	1.00	1.27	0.45	0.05	0.35 Ref.	0.70	4.20	4.20	0.261	C0.35	R0.20	0.05
Min.	4.90	5.90	0.90	BSC	0.35	0.00		0.50	4.00	4.00	0.195			0.00

The DC package option (8-DFN) is not recommended for new designs. Please select the DF (8-DFN small flag) option for new designs.

Figure 2 - DFN Small Flag Package



Dimension	A	B	C	D	E	F	G	H	I	J	K	L	M	N
Max.	5.10	6.10	0.90	1.27 BSC	0.45	0.05	1.60	0.70	2.10	2.10	.210	C0.45	R0.20	0.05
Min.	4.90	5.90	0.80		0.35	0.00	1.20	0.50	1.90	1.90	.196			0.00

Figure 3 - 8-pin SOIC (208 Mils) Package Outline

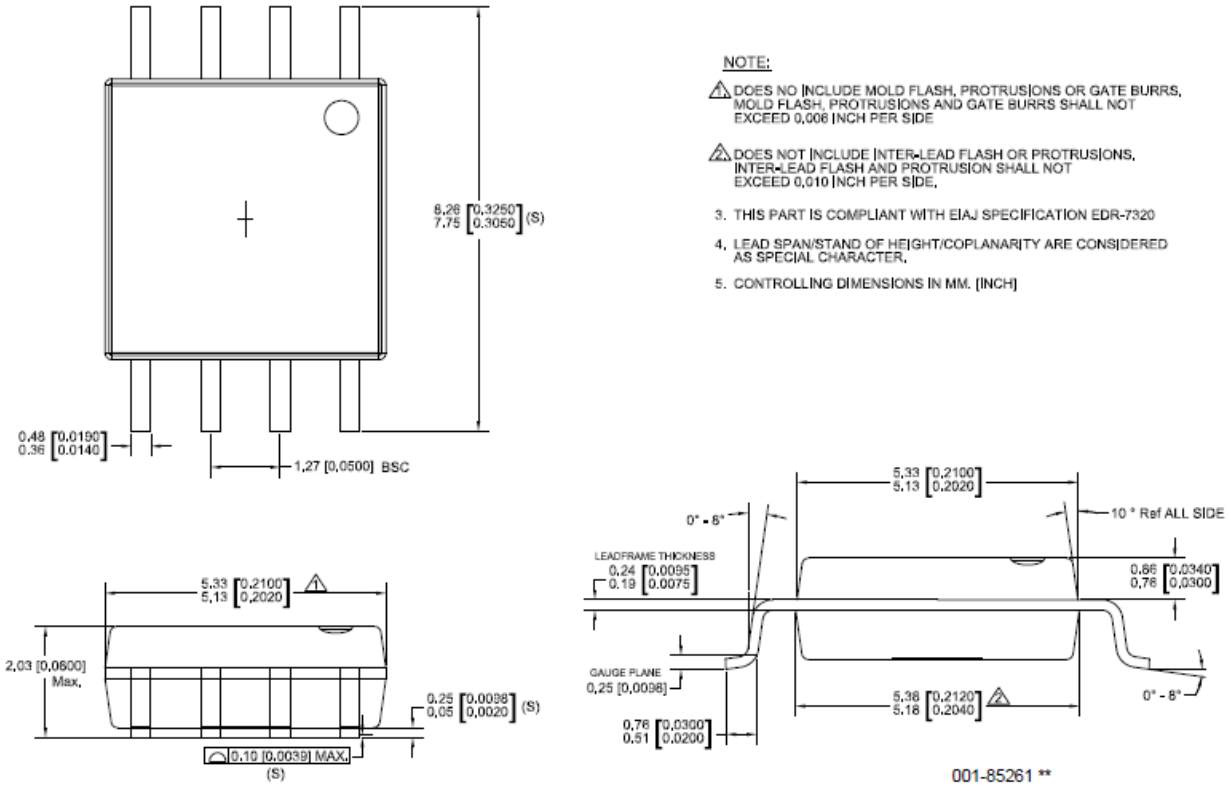
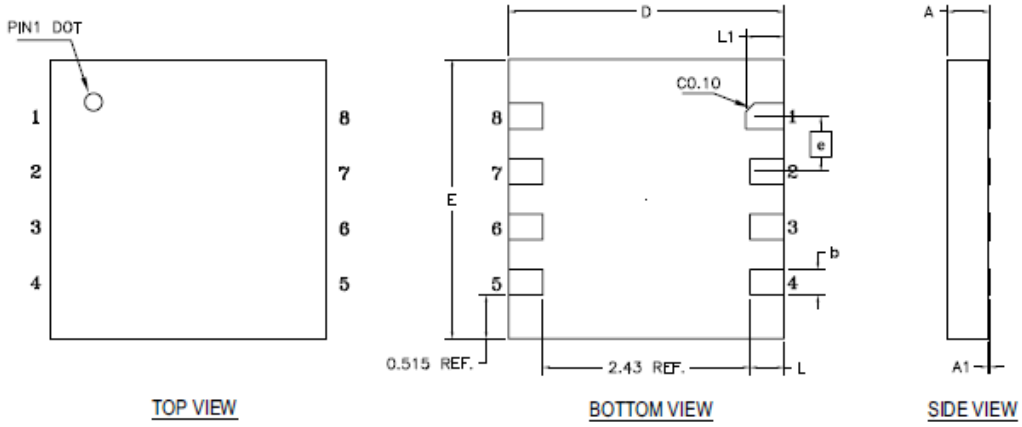


Figure 4 – 4 Mbit SPI F-RAM 8-pin GQFN (3.23 × 3.28 × 0.55 mm) Package Outline



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
e		0.65 BSC	
N		8	
L	0.30	0.40	0.50
L1	0.35	0.45	0.55
b	0.25	0.30	0.35
D	3.18	3.23	3.28
E	3.23	3.28	3.33
A	0.45	0.50	0.55
A1	0.00	-	0.05

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.

The SPI MRAM Exposed Metal Pad is not connected to the die, hence it should be left floating or connected to Vss. Ensure that the Exposed Metal Pad of the SPI MRAM DFN and Small Flag DFN package is not soldered on the PCB when migrating from SPI FRAM. Doing so will cause the SPI MRAM die to be exposed to excessive heat, which could result in bit failures and margin loss.

POWER CYCLE TIMING

Timing Parameters	Description	SPI MRAM (MR2xH40)	SPI F-RAM (CY15B104QN)	Comments
tDP/tENTHIB	Sleep mode entry time	3 µs	3 µs	Both devices take t_{DP} (3 µs) to enter sleep/Hibernate
tPU	Power-up VDD(min) to first access (CS LOW)	400 µs	450 µs (min)	Typically, the host controllers take longer than 400 µs to boot up. Systems must review the impact of longer t_{PU} time in the SPI FRAM and adjust their timing accordingly
t_{RDP} (t_{REC})	Recovery time from sleep	t_{RDP} = 400 µs	t_{REC} = 450 µs	Systems must review the impact of longer wake-up time of the SPI F-RAM and adjust their timing accordingly
t_{DIS} (t_{OD})	Output disable time	t_{DIS} = 12 ns (min)	t_{OD} = 12 ns (max)	The SPI FRAM defines this as max spec while the SPI MRAM defines this as min spec. The max spec ensures that the device will release the output within 12 ns. The min spec

				ensures that the device will release the output only after 12 ns. Providing the max spec is better for a system to determine when the bus will be available for access
tWPS (tCSU)	WP Setup To CS Low	tWPS = 5 ns (min)	tCSU = 5 ns (min)	Chip select setup
tWPH (tCSH)	WP Hold From CS High	tWPH = 5 ns (min)	tCSH = 5 ns (min)	Chip select hold - SPI mode 0
Power Parameters	**Description**	**SPI MRAM (MR2xH40)**	**SPI F-RAM (CY15B104Q)**	**Comments**
IOUT	DC output current per pin	±20 mA	±15 mA	This is the absolute maximum rating for the device. This parameter does not influence any device operation across its operating range
VWI	Write inhibit voltage	2.2 V	Not applicable	As soon as VDD falls below VDD min limit, the SPI MRAM writes are inhibited
tVR	VDD power-up ramp rate	Not specified	50 µs/V	Systems must ensure that VDD power-up ramp rate is within the datasheet spec
tVF	VDD power-down ramp rate	Not specified	100 µs/V	Systems must ensure that VDD power-down ramp rate is within the datasheet spec

Figure 5 - Mbit SPI MRAM Power Cycle Timing

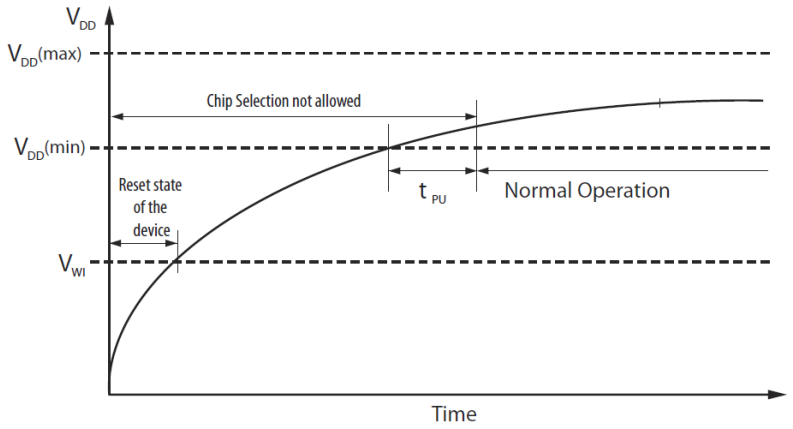
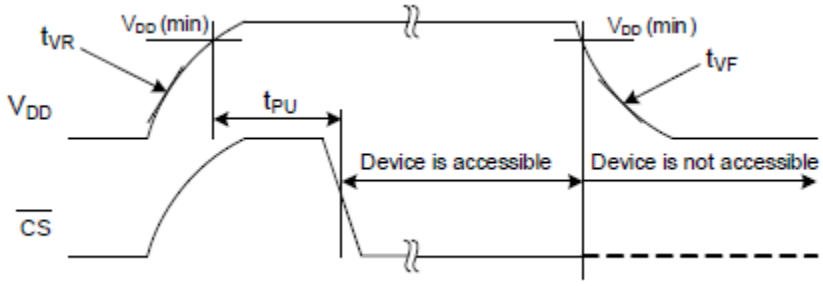


Figure 6 - Mbit SPI FRAM Power Cycle Timing



Command (OPCODE) Compatibility

Command OPCODE (Hex)	Command Description	SPI MRAM (MR2xH40xDF)	SPI F-RAM (CY15B104QN)	Comments
WREN (06h)	Write Enable	√	√	Identical functionality
WRDI (04h)	Write Disable	√	√	Identical functionality
RDSR (05h)	Read Status Register	√	√	An RDSR command cannot immediately follow a READ command. If an RDSR command immediately follows a READ command, the output data will not be correct. Any other sequence of commands is allowed. If an RDSR command is required immediately following a READ command, it is necessary that another command be inserted before the RDSR is executed. Alternatively, two successive RDSR commands can be issued following the READ command. The second RDSR will output the proper state of the Status Register
WRSR (01h)	Write Status Register	√	√	Identical functionality
READ (03h)	Read Data Bytes	√	√	Identical functionality
FSTRD (0Bh)	Fast read memory data	X	√	The 4-Mbit SPI MRAM doesn't support this command
SSWR (42h)	Special Sector Write	X	√	The 4-Mbit SPI MRAM doesn't support this command
SSRD (4Bh)	Special Sector Read	X	√	The 4-Mbit SPI MRAM doesn't support this command
WRITE (02h)	Write Data Bytes	√	√	Identical functionality
SLEEP/HBN (B9h)	Enter sleep mode	√	√	Both memory take 3us before entering sleep mode
DPD (B9h)	Enter Deep Power Down	X	√	The 4-Mbit SPI MRAM does not support this feature
WAKE (ABh)	Exit sleep mode	√	X	The 4-Mbit SPI F-RAM does not support this command. Migrating from MRAM to F-RAM does not require any software update because the SPI F-RAM wakes up when $\overline{CS}$ toggles HIGH to LOW and ignores the subsequent WAKE instruction sent on its input
RDID (9Fh)	Read device ID	X	√	The 4-Mbit SPI MRAM does not support this feature
RUID (4Ch)	Read Unique ID	X	√	The 4-Mbit SPI MRAM does not support this feature
WRSN (C2h)	Write Serial Number	X	√	The 4-Mbit SPI MRAM does not support this feature
RDSN(C3h)	Read Serial Number	X	√	The 4-Mbit SPI MRAM does not support this feature

Status Register Compatibility

The Status Register access in the case of the 4-Mbit SPI MRAM and the SPI F-RAM are identical. However, the value returned by the Status Register read can differ between the two parts for some bit locations. For example, the "Don't Care" bits in the SPI MRAM Status Register are writeable and they can return either '0' or '1', while the "Don't Care" bits in the SPI F-RAM Status Register are read-only bits and always return '0'. Table below shows the Status Register bits definition for the two parts and their compatibilities.

Status Register	SPI MRAM (MR2xH40xDF)	SPI F-RAM (CY15B104QN)	Comments
Bit0	Don't Care	Don't Care (0)	This bit is non-writeable in the SPI FRAM and always returns '0' upon read. This bit can be modified in the SPI MRAM
Bit1	WEL	WEL	Identical behavior
Bit2	BP0	BP0	Identical behavior
Bit3	BP1	BP1	Identical behavior
Bit4	Don't Care	Don't Care (0)	These bits are read-only in the SPI F-RAM and always return '0' upon read. These bits can be modified in the SPI MRAM
Bit5	Don't Care	Don't Care (0)	
Bit6	Don't Care	Don't Care (1)	This bit is the read-only bit in the SPI FRAM and always returns '1' upon read. This bit can be modified in the SPI MRAM
Bit7	SRWD	WPEN (0)	Identical behavior

Device Spec Compatibility

Everspin device is a 40 MHz/50MHz MRAM that operates at 2.7V - 3.6V, with a nominal Vdd = 3.3V, while the SPI-FRAM has a wider operating voltage range (1.8V to 3.6V). There are a few parameters that warrant some system level analysis before replacing the SPI-FRAM with the SPI-MRAM, including output load, start-up time and power up and power down ramps.

RELIABILITY CONSIDERATIONS FOR COMPARISON

The CY15B104QN FRAM architecture employs ferroelectric materials as storage devices. These materials have an intrinsic electric dipole switched into opposite polarities with an external electric field. A read operation in a FRAM is destructive because it requires switching the polarization state in order to sense its state. The read operation has to restore the polarization to its original state after the initial read which adds cycle time to the read operation. FRAM Read and Write cycles require an initial "Pre-charge" time which can increase the initial access time. Ambient operating temperatures above 85°C accelerate wear-out of FRAM due to build-up of free electric charge resulting in imprint.

Everspin MRAM will provide the most cost-effective non-volatile RAM solution. MR2xH40xDF MRAM is built using a much simpler 1-transistor, 1-magnetic tunnel junction cell. The simple Everspin MRAM cell leads to improved manufacturing efficiency and increased reliability. MRAM uses magnetic tunnel junction technology for non-volatile storage. Data does not leak away at high temperature and there is no wear-out mechanism to limit the number of read, write, or power cycles in this technology. Another important aspect of the reliability of toggle MRAM is the data retention against errors from thermally induced magnetization flips. Accelerated baking tests were conducted in which checkerboard patterns were written into the parts before the bake and the data was read back afterwards. The 1500 representative 4-Mb parts across three lots were baked under conditions ranging from 2000 h at 150 C to 2 h at 260 C and zero data retention flips were observed for all the parts. Extrapolation back to operating temperatures indicates a data retention lifetime exceeding 20 years. MRAM also offers radiation-hard performance due to the inherent robustness of the magnetic materials to radiation exposure. Alpha particle and neutron irradiation of 4-Mb dies showed an error rate of <0.5 FIT/Mb.

MRAM MAGNETIC TOLERANCE

Everspin Technologies SPI MRAMs provide low susceptibility to data corruption when operated in magnetic field environments, therefore helping engineers to design high magnetic tolerance reliable systems. The maximum external magnetic field that can be applied to SPI MRAMs is 12000 A/m (150 Gauss), during write, read and standby operations. Everspin Technologies provide specific guides about how to operate MRAMs in these situations.

SUMMARY

Replacing a CY15B104QN with Everspin's MR2xH40xDF 4Mb SPI MRAM is a straight-forward process. These devices are functional equivalent with some hardware and software considerations of pinout, power supply and timing details shown in this application note.

Table 2 – MRAM Ordering Part Numbers

Speed Grade	Temp Grade	Tempera-ture	Package	Shipping Con-tainer	Order Part Number
50MHz	Industrial	-40 to +85 C	8-DFN Small Flag	Trays	MR20H40CDF
				Tape and Reel	MR20H40CDFR
40 MHz	Industrial	-40 to +85 C	8-DFN [1]	Trays	MR25H40CDC [1]
				Tape and Reel	MR25H40CDCR [1]
			8-DFN Small Flag	Trays	MR25H40CDF
				Tape and Reel	MR25H40CDFR
	Extended	-40 to +105 C	8-DFN Small Flag	Trays	MR25H40VDF
				Tape and Reel	MR25H40VDFR
	AEC-Q100 Grade 1	-40 to +125 C	8-DFN Small Flag	Trays	MR25H40MDF
				Tape and Reel	MR25H40MDFR

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