Replacing the Fujitsu MB85R8M2T FRAM with Everspin's MR3A16ACMA35 MRAM

EVERSPIN MRAM MEMORY

Everspin is the worldwide leader in designing, manufacturing, and commercially shipping discrete Magnetoresistive RAM (MRAM) into markets and applications where data persistence and integrity, low latency, and security are paramount.

RELIABLE SUPPLY

Everspin is a long term, reliable manufacturer of MRAM products and operates a fabrication facility in Chandler, Arizona.

SUMMARY

The Everspin's 8Mb MRAM MR3A16ACMA35 can operate with the Fujitsu 8Mb FRAM MB85R8M2T slower timing, but also allows the system designer to take advantage of MRAM's four times faster random access cycle time. The Everspin 8Mb MRAM MR3A16ACMA35 is available in 48 Pin BGA package.

BENEFITS OF MR3A16ACMA35

Upgrading to Everspin MRAM provides many benefits over Fujitsu FRAM:

- Faster Random Access Operation Times
- High Reliability and Data Retention
- Unlimited Read/Write Endurance
- No Wear-out Concern
- Competitive Pricing
- Stable Manufacturing Supply Chain
- Small Footprint BGA Package

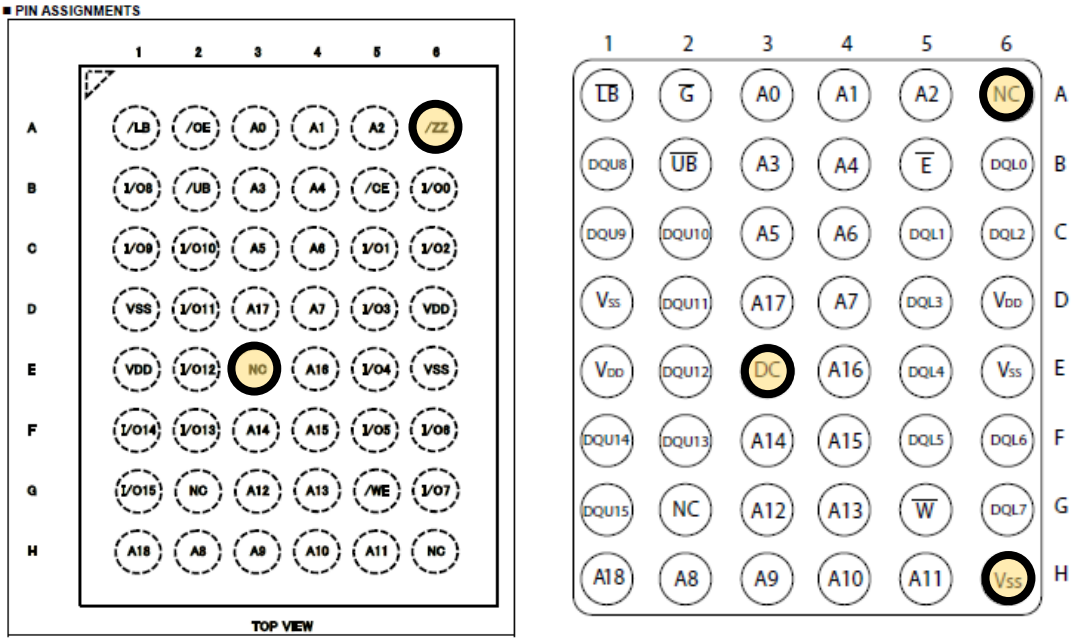
COMMON PINS

The MR3A16ACMA35 is an 8Mb non-volatile RAM organized as 512kx16 operating from a nominal 3.3V power supply and is compatible with FRAM. Both products use standard SRAM parallel address (A0-16), byte-wide bidirectional data pins (DQ0-7) and control signals (/E, /W, /G). Each can be supported by a common timing interface and will function as random access read/write memories that retain data without external battery when power is removed. Everspin does not support the /ZZ sleep function. /ZZ may require pull-up.

Table 1 – Overview: MB85R8M2TPBS vs. MR3A16ACMA35

Parameter	MB85R8M2TPBS-M-JAE1	MR3A16ACMA35
Package	48 Ball BGA	48 Ball BGA
Size and Height	6 × 8 × 1.2 mm	10 x 10 x 1.27 mm
Pinout / Footprint	See Figure 1 and Table 2 below	
Solder Profile	Per JEDEC J-STD-020D.1	

Figure 1 – Pinout/Footprint Comparison and Considerations



Fujitsu **Everspin Technologies**

Table 2 – Pin Function Comparison

Ball #	Fujitsu	Everspin	Everspin Definition	Everspin Comments
A6	/ZZ	NC	No Connection	Function of /ZZ is not available on the Everspin device. Recommend to float or pull low.
E3	NC	DC	Do Not Connect	This pin is used for test. Recommend to float. If driven, must be pulled to V_{IL}.
H6	NC	Vss	Ground	

MRAM PROVIDES FASTER TIMING

The MR3A16ACMA35 and MB85R8M2T use address, data, and control signals that are similar to standard SRAM. The Everspin MR3A16ACMA35, however, allows for faster read and write operations at 35ns. The Fujitsu FRAM requires a read cycle time of at least 150ns for random read accesses. The internal operation of the MB85R8M2T requires a precharge time of at least 75ns following a 75ns initial read access, resulting in a random access minimum cycle time of 150ns. The pre-charge time is present whether self-timed by the part or initiated by the user by bringing /CE high. FRAM performs the read during the initial access portion of the cycle time and then restores the data to the memory cell (writes data back) during the pre-charge time like a DRAM. This is known as destructive readout operation. MRAM can operate with this slower FRAM read sequence but MRAM is actually much faster as it does not have a destructive read mechanism. Both read and write cycles wear out the FRAM. MRAM has unlimited read and write endurance. The MR3A16ACMA35 supports a 35-ns read access and cycle

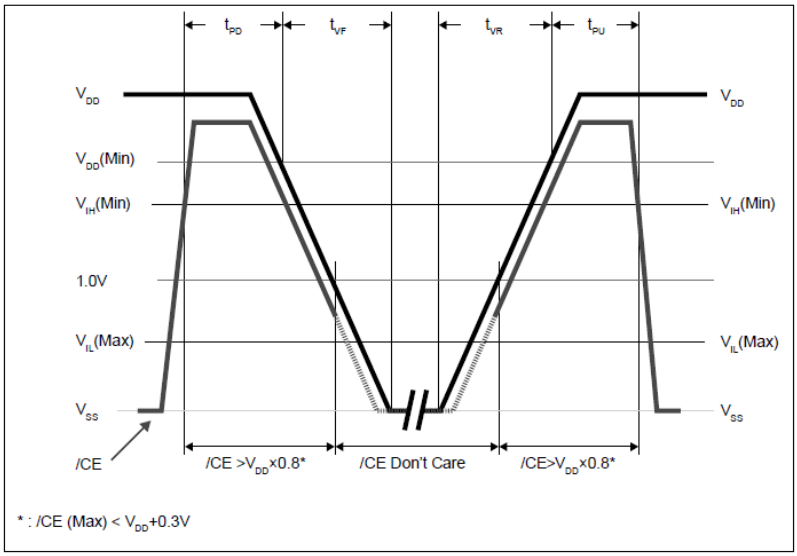
time. The MR1A16ACMA35 does not require a precharge cycle and is two times faster than the FRAM on initial read access time and four times faster on random accesses. The FRAM requires 150ns to complete a write cycle just as it does a read cycle. The MRAM will operate with this timing but actually has a write cycle time of just 35 ns (4 times faster than FRAM). To take advantage of the four times faster random read and write speed of the MR3A16ACMA35, you may wish to modify the control interface. MRAM plugs directly into most SRAM controllers without change.

POWER CYCLING CONSIDERATIONS

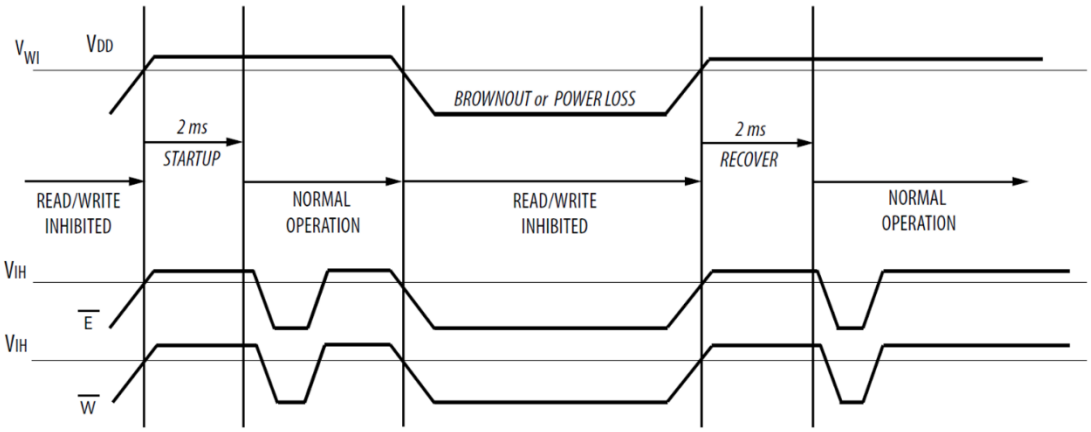
The MB85R8M2T has a power startup time of 450 us and a power down time of 85 ns, while the MR3A16ACMA35 is specified at 2ms for power up and power down sequences. These differences in startup times will not be an issue in most system designs since the power-up master reset is purposely made much longer to assure that all circuitry is stabilized for start of operation.

Figure 2 Power Up and Power Down Diagrams

FRAM Timing



MRAM Timing



POWER SUPPLY CONSIDERATIONS

Both the MRAM and the FRAM are specified at nominal 3.3V power supply. The FRAM has a standby current of 300 uA. To enable three times faster random access speed, MRAM's standby current is 9 mA. For battery-powered applications , designers can take advantage of MRAM's non-volatility and power gate the MRAM to reduce standby power to zero when not in use.

READ AND WRITE CURRENTS

The read and write current for the MR3A16ACMA35 is similar to the MB85R8M2T at 20 mA active current for 150 ns cycle time. MR3A16ACMA35 is specified at 60 mA read, 152 mA write when operating at its faster 35 ns cycle time operation.

RELIABILITY CONSIDERATIONS FOR COMPARISON

The MB85R8M2T FRAM architecture employs ferroelectric materials as storage devices. These materials have an intrinsic electric dipole switched into opposite polarities with an external electric field. A read operation in a FRAM is destructive because it requires switching the polarization state in order to sense its state. The read operation must restore the polarization to its original state after the initial read which adds cycle time to the read operation. FRAM Read and Write cycles require an initial "Pre-charge" time which can increase the initial access time. Ambient operating temperatures above 85°C accelerate wear-out of FRAM due to build-up of free electric charge resulting in imprint.

Everspin MRAM will provide the most cost-effective non-volatile RAM solution. MR3A16ACMA35 MRAM is built using a much simpler 1-transistor, 1-magnetic tunnel junction cell. The simple Everspin MRAM cell leads to improved manufacturing efficiency and increased reliability. MRAM uses magnetic tunnel junction technology for non-volatile storage. Data does not leak away at high temperature and there is no wear-out mechanism to limit the number of read, write, or power cycles in this technology. Data retention is better than 20 years at 125°C.

SUMMARY

Replacing a MB85R8M2T with Everspin's MR3A16ACMA35 2Mb MRAM is a straight-forward process. These devices are close to a drop-in replacement with some consideration of pinout, package size and timing details shown in the application note.

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