Replacing the Cypress CY14B108N nvSRAM with Everspin's MR3A16Axxx35 MRAM

GENERAL CONSIDERATIONS FOR REPLACING NVSRAM WITH MRAM

Every write with an MRAM is instantly non-volatile for at least 20 years. There is no transfer of data from a volatile to a non-volatile memory cell, no external capacitors or back up batteries. The elimination of external components, highly reliable data retention, and 35ns SRAM compatible READ/WRITE Access times make the Everspin MRAM a viable candidate for replacing the Cypress CY14B104NA-BA/ZS45XI nvSRAM without compromising system performance.

EVERSPIN MRAM MEMORY

Everspin is the global leader in commercially viable MRAM technology and Everspin MRAM products are present in hundreds of applications demanding high-speed, reliable, non-volatile memory.

MR3A16A comparison to CY14B104NA

The Everspin MRAM solution provides:

- Always Non-Volatile. No Unreliable Capacitor Dependent Backup Cycles
- No Vcap or Vbatt required
- Immediate (<1ns) Power-off with no loss of data
- No complex Software STORE/RECALL routines
- Fast Start-up time (2ms vs. 20ms)
- Unlimited Read and Write cycles - No Wear-out Concerns
- 20-Year Data Retention with No Cycling Dependence
- Fewer components means smaller design footprint and lower total BOM cost
- Directly replaces the Cypress nvSRAM

COMPATIBILITY

The Everspin MR3A16AxYS35 (54-TSOP2) and MR3A16AxMA35 (FBGA) memories are pin, timing, and package compatible with the Cypress CY14B108N-ZS and CY14B108N- BA nvSRAM's respectively.

TIMING COMPATIBILITY

Both Everspin MRAM and nvSRAM have standard, compatible asynchronous SRAM timing. The MRAM however, retains data even at power off for an indefinite period of time and over temperature cycling. With a 35 ns read/write cycle time, the MRAM is compatible with similar nvSRAM speed grade options.

It is important to note that the Everspin MR3A16Axxx device requires a minimum of 12ns hold time from Write Enable (and Chip Enable) high to Address invalid (Please see T_{WHAX} and T_{EHAX} in the MR3A16A data sheet available here.) Most microprocessors can accommodate this Hold time.

PIN COMPATIBILITY

- 8Mb organized in the 512Kx16 configuration
- 3.3 volt nominal operation
- Standard SRAM parallel address pins (A0-18)
- Standard byte-wide, bidirectional data pins (DQ0-15)
- Standard control signals (/E, /W, /G)

The MR3A16Axxx does not require an external capacitor and the other associated passive components required by the CY14B108N-xx devices.

Tables 1 and 2 highlight the differences in signal name and function for the Everspin and Cypress components. The primary difference between the Cypress and Everspin devices are the two pins on the nvSRAM: VCAP and /HSB. These pins are used to support the nvSRAM backup cycle and are not required for operation of the MRAM.

V_{CAP} pin

A capacitor is required on the V_{CAP} pins (Pin 36 on the TSOP2 and Ball E3 on the FBGA) on nvSRAM devices. Everspin assigns a "Do not connect" (DC) to the corresponding pin on the TSOP package and "No Connect" to the corresponding pin on the FBGA package. When replacing the Cypress nvSRAM with the Everspin MRAM, it is recommended that this pin be either left floating or kept at to V_{ss}.

/HSB pin

The /HSB pin of the nvSRAM (Pin 54 on the TSOP2 and Ball G2 on the FBGA) is used to either initiate a Hardware Store or indicate a Hardware Store is in process. The corresponding pin on the Everspin MRAM is labeled as "No Connect". Therefore, a Host processor should not expect the MRAM to drive this pin to a particular voltage level.

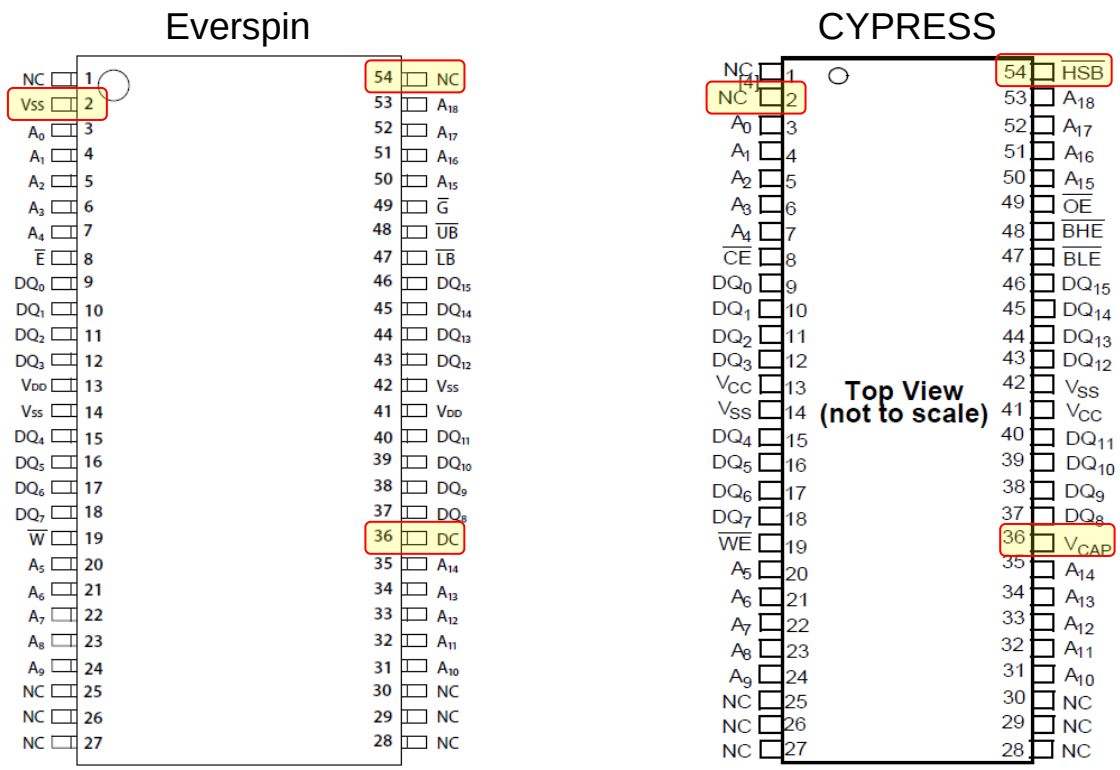


Figure 1 - Pinout comparison between MRAM and nvSRAM, 54 pin TSOP2 package

PIN #	Everspin	Cypress	Everspin connection	Everspin Comments
36	DC	VCap	Do Not Connect	This pin is used for test. Prefer to float. If driven, must be pulled to V_{IL}. Do not place nvSRAM capacitor.
54	NC	HSB#	Not connected	This pin is not connected to the die. It is the designer's responsibility to ensure compatibility
2	Vss	NC	Vss/GND	Vss/GND pin. The voltage on this pin must not exceed V_{IL}

Table 1- Pin function comparison between MRAM and nvSRAM, 54 pin TSOP2 package

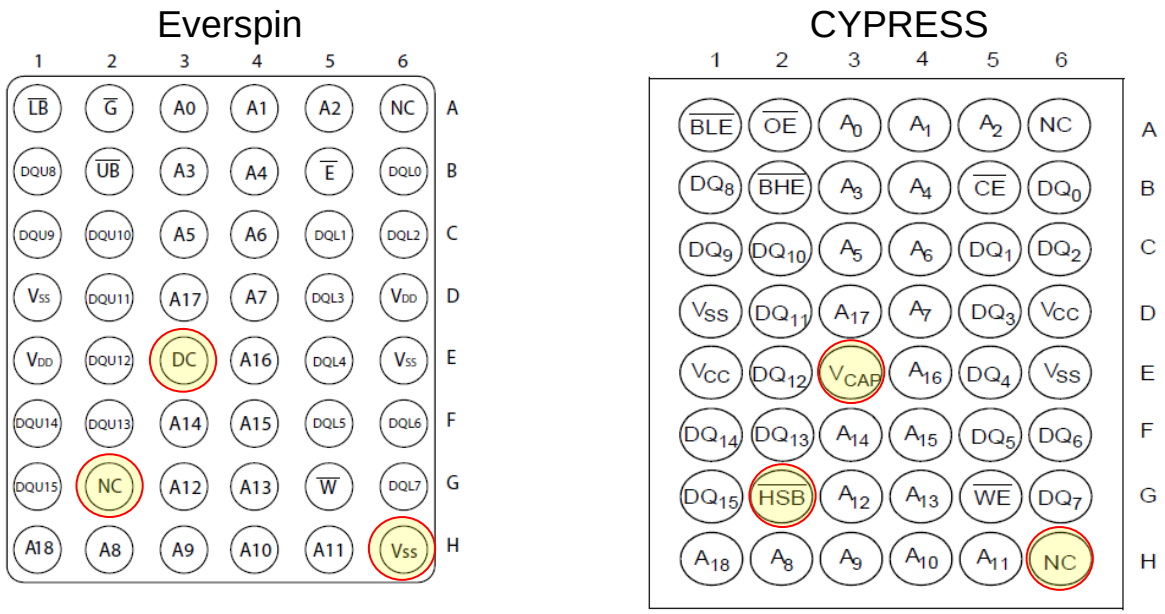


Figure 2 - Pinout comparison between MRAM and nvSRAM, 48 FBGA package

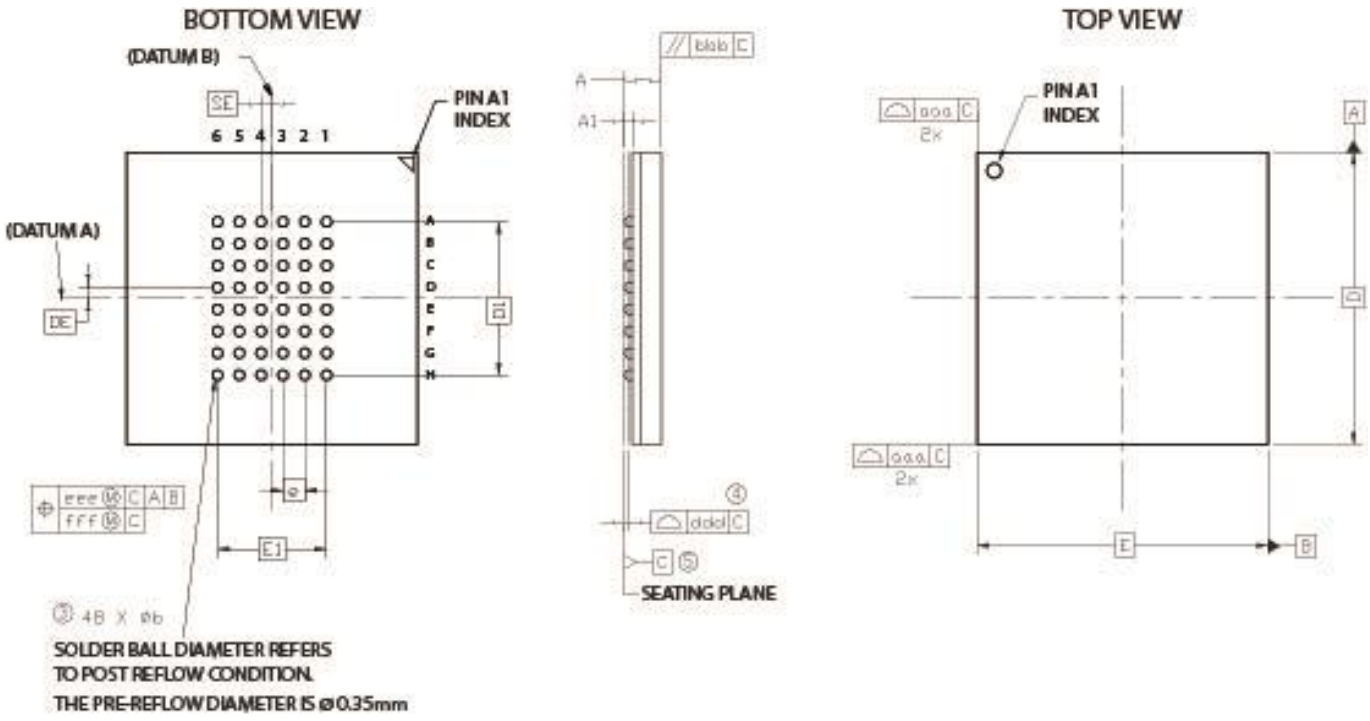
PIN #	Everspin	Cypress	Everspin connection	Everspin Comments
E3	DC	VCap	Do Not Connect	This pin is used for test. Prefer to float. If driven, must be pulled to VIL. Do not place
G2	NC	HSB#	Not connected	This pin is not connected to the die. It is the designer's responsibility to ensure compatibility with the system design
H6	Vss	NC	Vss/GND	Vss/GND pin. The voltage on this pin must not exceed VIL

Table 2 - Pin function comparison between MRAM and nvSRAM, 48 FBGA package

PACKAGE COMPATIBILITY

The Everspin 54 pin TSOP2 and FBGA devices are drop-in compatible with the corresponding Cypress equivalents. However, see figures 3 and 4 to understand the package dimension differences between the Cypress and Everspin FBGA packages. Make special note of the package dimension differences requiring different mechanical "Keep out" areas for these packages. Please refer to the current datasheet for details.

EVERSPIN FBGA PACKAGE DIMENSION



Ref	Min	Nominal	Max
A	1.19	1.27	1.35
A1	0.22	0.27	0.32
b	0.31	0.36	0.41
D		10.00 BSC	
E		10.00 BSC	
D1		5.25 BSC	
E1		3.75 BSC	
DE		0.375 BSC	
SE		0.375 BSC	
e		0.75 BSC	

Figure 3

NVSRAM FBGA PACKAGE DIMENSION

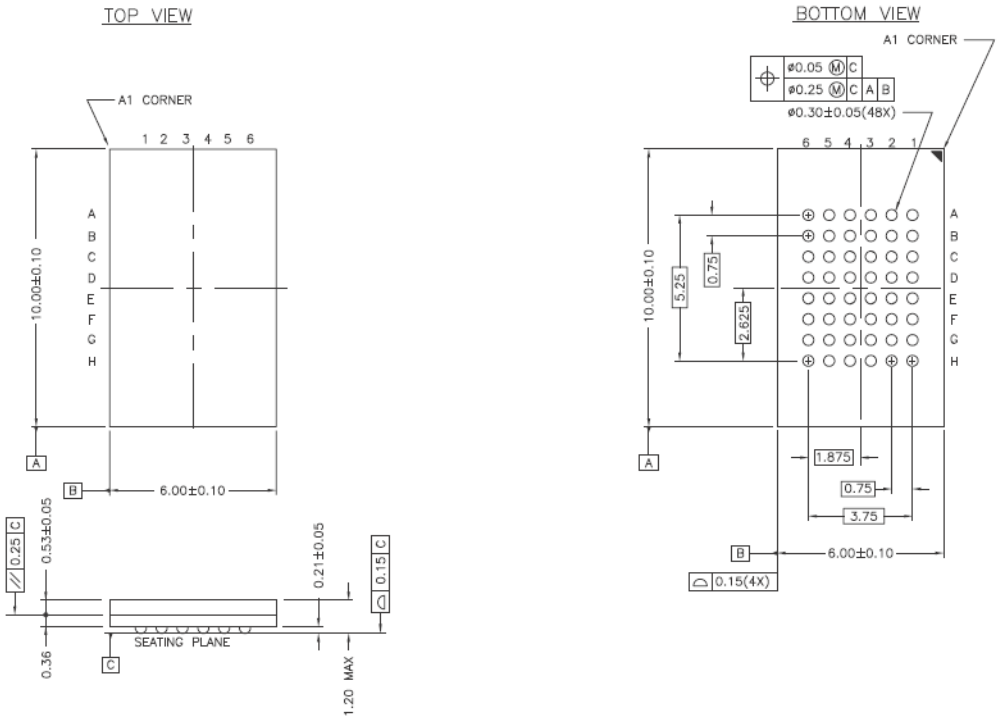


Figure 4

OTHER REPLACEMENT DESIGN CONSIDERATIONS

HSB SOFTWARE

Due to its persistence, there is no power monitoring requirement for the Everspin MRAM as is the case with the nvSRAM. Hence initiating or monitoring Hardware Stores, Re-stores and associated software routines are unnecessary and can be eliminated.

SIMPLIFIED POWER CYCLING

When power is removed from the MRAM, data remains valid over 20 years' time and across the temperature range. This feature, unique to MRAM, allows for Duty Cycle Power control enabling the user to reduce their overall power consumption without concern of wear-out or lost data.

MRAM requires control signals /E and /W to track the power supply during power-up and be held high for a 2 ms start-up period a much shorter power-up requirement than the nvSRAM. When power fails, the Everspin MRAM simply inhibits write operations and no special power down timing considerations are needed

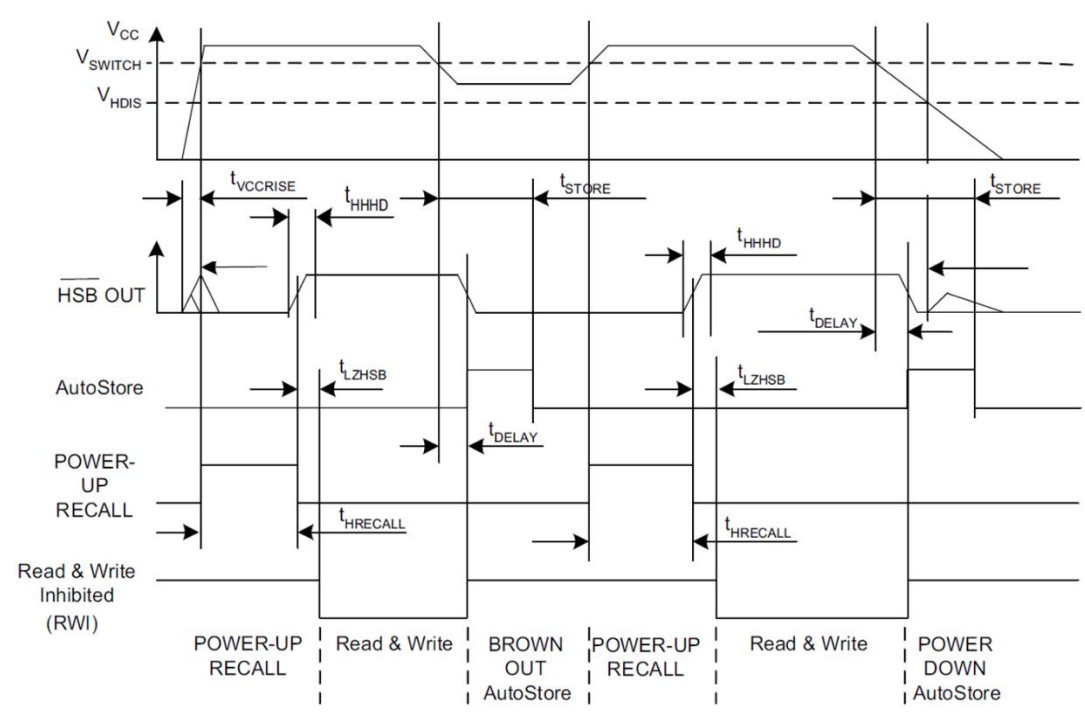
since data is always non-volatile.

The nvSRAM device requires the /WE signal to track the power supply during power-up and be held high during the power-up recall period of 20 ms. The nvSRAM must sense the power failure, decouple the power supply from its backup capacitor, wait for any SRAM operations to complete, and then perform a parallel write to the EEPROM storage element during the 8 ms period after power has failed. This sequence is complicated by the fact that power falls at various ramp rates and in some cases bounces above and below the power supply threshold (brown outs) in rapid succession. Such conditions are not easily simulated or tested raising concerns about reliability of the backup storage cycle and the data in the EPROM.

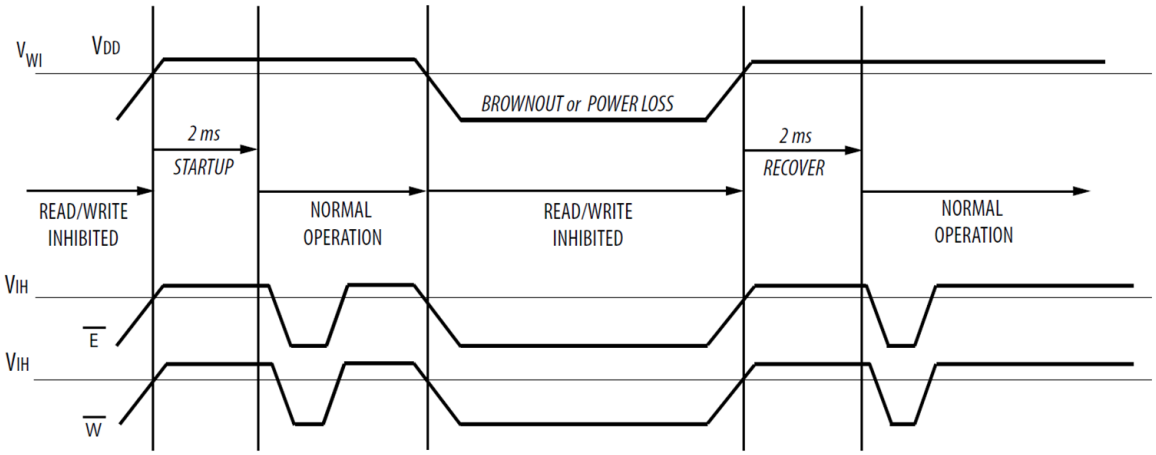
POWER-UP SEQUENCING

Both MRAM and nvSRAM will operate from a standard +3.3 V power supply with +/-10% power supply range. Both MRAM and nvSRAM have similar standby and active operating currents, however, the "Start-up" time for the MRAM is 2ms vs. 20ms for the nvSRAM. Proper decoupling capacitors should be used to assure reliable operation. The power loss/startup sequences for both products are shown below:

nvSRAM Timing



MRAM Timing



RELIABILITY CONSIDERATIONS FOR COMPARISON

The CY14B108N-xx uses conventional trapped charge technology for non-volatile storage. Data can leak away as wear-out results from temperature and excessive write cycles.

Everspin MRAM will provide the most cost-effective non-volatile RAM solution. The nvSRAM is constructed by combining a standard 6-transistor SRAM with a non-volatile EEPROM storage element in every cell. The total cell complexity is 12-transistors. MR3A16Axxx is built using a much simpler 1-transistor, 1-magnetic tunnel junction cell. The simple Everspin MRAM cell leads to improved manufacturing efficiency and increased reliability.

The reliability of an nvSRAM is dependent upon not only the memory chip but also the quality of the external VCAP capacitor. Careful capacitor selection is necessary to assure reliable power sequencing.

MRAM uses magnetic tunnel junction technology for non-volatile storage. Data does not leak away at high temperature and there is no wear-out mechanism to limit the number of read, write, or power cycles in this technology. Data retention is better than 20 years at 125°C.

SUMMARY

Replacing a CY14B108N-xx with Everspin's MR3A16Axxx 8Mb MRAM is a straight-forward process. These devices are close to a drop-in replacement with some consideration of pinout and timing details shown in the application note.

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