Application Note

ST-DDR4 Design Guide For Xilinx FPGA Controllers

1. Introduction

Spin-Transfer Torque Magneto-resistive Random Access Memory (STT-MRAM) is a persistent memory technology that delivers performance, persistence, and durability utilizing variants of industry standard interfaces. Everspin has introduced STT-MRAM products that utilize a variant of the JEDEC standard DDR4 interface, called ST-DDR4, that encompasses the unique functionality required for full system support. This document will help engineers understand how to enable a Xilinx FPGA memory controller to communicate with persistent ST-DDR4 memory.

2. Enabling ST-DDR4

To enable designers a fast path to integration of ST-DDR4 support, the process starts with an existing 8Gb DDR4 SDRAM-2666 Memory Interface Generator (MIG) that is generated from the Xilinx Vivado development environment. The deviations from the 8Gb DDR4 SDRAM are as follows and will be explained in subsequent sections:

1. Timing (reduce operating frequency, increase row access timing, increase counter widths and reduce CAS page sizes)
2. Power-up (calibration – anti-scribble mode enabled during calibration)
3. Power-down (scramming or moving all relevant data into the persistent memory array)
4. Performance (increase pipeline depth and increase data transfer efficiency)

Note: Also required for a robust ST-DDR4 persistent memory design, but outside the scope of this document, is implementation of a system level Error Correction Code (ECC) scheme.

3. DDR4 SDRAM-1333 Memory Interface

In the Xilinx design environment, the DDR4 interface logic will be generated based upon input parameters that represent the speed and timing characteristics of an 8Gb SDRAM DDR4-2666. Since the MIG cannot create interface logic using parameters outside of the current JEDEC standard, a JEDEC compatible DDR4 controller must be created as a preliminary first step. The Everspin 1Gb ST-DDR4 1333 device most closely resembles a 8Gb DDR4-2666 SDRAM device, therefore use the timing values from the 8Gb DDR4 SDRAM 2666 spec SDRAM DDR4-2666 (Table 145, Timing Parameters Used for IDD Measurements – Clock Units, please reference the DDR4-2666 part only). Once the DDR4 interface logic has been created, the timing, power-up, power-down and performance parameters can be modified to enable ST-DDR4 persistent memory.

It is highly recommended after creating a MIG, an example testbench be created in Vivado by right clicking on the .xci file and selecting the menu item called "Open IP Example Design...". Creating an example design will create a new Vivado project with all the test files required to simulate your newly created MIG. See the Xilinx MIG creation tutorial Designing a Memory Interface and Controller with Vivado MIG for UltraScale and the Memory Interfaces Design Hub - UltraScale DDR4/DDR4 Memory.
Note: All MIG creation and changes referenced in this document were performed using Vivado 2018.3.

4. Xilinx FPGA Controller Modifications Explained

The changes required to the existing Xilinx MIG DDR4 controller to enable ST-DDR4 operation as mentioned earlier is categorized as Power-up, Timing, Power-down, and Performance modifications. Each category will be explained in detail below.

4.1 Power-up

For a detailed Power-up sequence for DDR4 STT-MRAM, please refer to the EMD4E00GAS2 Datasheet available on the Everspin website. Briefly there are two main areas to consider for Power Up Sequencing: Default Mode Register Values, and Power Up Signal Levels.

Mode Register Settings

Full Mode Register compatibility is supported and should be set as follows during power-up initialization or after a reset for proper ST-DDR4 1333 operation. Mode Register programming should be performed in the following sequence:

1. Mode Register 0 (MR0) – 14'b10_0001_0000_0100
2. Mode Register 1 (MR1) – 13'b0_0000_0000_0101
3. Mode Register 2 (MR2) – 13'b0_0000_0000_0000
4. Mode Register 3 (MR3) – 13'b0_0001_1000_0000
5. Mode Register 5(MR5) – 13'b0_0100_1110_0000
   After Calibration and before normal operation
6. Mode Register 0 (MR0) – 14'b00_0000_0000_0100

Note: Ensure MR0[13] is set to 1 before calibration in order to put the STT-MRAM device in NOMEM mode. This prevents data corruption during write leveling. This is also referred to as anti-scribbling. Since STT-MRAM is persistent memory, writing to locations during calibration might overwrite known good data, thus the function of NOMEM mode. Before normal operation, it's important to set MR0[13] = 0 in order to disable NOMEM mode and allows accesses to the persistent memory array.

Power Up Signal Levels

Power up signal levels is beyond the scope of this document and requires the user to refer to the EMD4E00GAS2 Datasheet.

4.2 Timing

As mentioned above, the timings of the ST-DDR4 are modified from a known good Xilinx generated DDR4 SDRAM MIG. The key timing parameters for both the original DDR4 SDRAM and the ST-DDR4 MRAM are listed in **Table 1** below.

In conjunction to the time parameters in **Table 1**, corresponding column and counter width changes are also required. These are outlined in **Table 2** below.

Table 1 - Table showing key timing parameters for DDR4 and ST-DDR4

Parameter	***Symbol***	***DDR4-2666 SDRAM***		***ST-DDR4-1333 STT-MRAM***	
		ns (min)	***ck (min)***	***ns (min)***	***ck (min)***
Clock Period	*tCK*	0.75		1.2	
Cas Latency	*CL*		18		10
Cas Write Latency	*CWL*		7		9
Column to Column command delay	*tCCD*		4		4
Internal READ to first data	*tAA*	13.50	18	15	10
ACTIVE to internal READ or WRITE delay time	*tRCD*	13.50	18	135	90
Precharge command period	*tRP*	13.50	18	7.5	5
ACTIVE to ACTIVE command period	*tRC*	tRAS + tRP		150	100
ACTIVE to Precharge command period	*tRAS*	36	24	143	96
Write Recovery, WRITE to Precharge delay time	*tWR*	15	10	15	10
ACT to ACT Command Period, different banks	*tRRD*	6	4	10	
Four ACTIVE Window	*tFAW*	30	20	240	160
REFRESH to ACT command delay (1Gb to 8Gb)	*tRFC*		74 – 234	*Must equal tST*	
Store Operation period	*tST*	-	-	380	254

Table 2 - Column Width and Counter Differences for ST-DDR4

Parameter (bits)	***JEDEC DDR4***	***1Gb ST-DDR4***
IO Width	x8	x8, x16

Page size	8192	1024(x8), 2048 (x16)
tRASf	3	7
TXN_FIFO_DEPTH	4	16
TXN_FIFO_PWIDTH	2	4
CAS_FIFO_DEPTH	4	16
CAS_FIFO_PWIDTH	2	4
trcd_cntr / trcd_cntr_nxt	4	7
trp_cntr	5	7
tras_cntr_rb / tras_cntr_rb_nxt	4	7
Column Address Width (bits)	$A_0 – A_9$ (10)	$A_0 – A_6$ (7)

Please use **Table 1** and **Table 2** as a check to ensure all timing changes match those generated in the modified ST-DDR4 MIG.

4.3 Power-down (Scram)

Scram is not a command, or an opcode. Scram is a power down procedure. It literally means power is going away, so the controller needs to guarantee persistence of all open pages and buffers by writing them to the persistent array. **This is true whether it is a planned power down or an unexpected power event.** If the event is unexpected, Scram needs to happen as quickly as possible. In most cases "as quickly as possible" is within 10 microseconds, but this timeframe is design dependent and should be calculated, simulated, and measured to guarantee all important data is written to the persistent memory array. To guarantee persistence, executing a REFRESH command is necessary to move data into the persistent memory array.

Note: In some designs that use both DRAM/MRAM and the DRAM capacity exceeds the size of the MRAM capacity, the controller needs to always guarantee (during normal operation) that important data that requires persistence and residing in DRAM never exceeds the size of the MRAM array.

Below is the scramming procedure:

1. The controller has been told to shut down or detects that the input supply voltage (usually +12Vdc) is either slumping, over-voltage, over-current, or an over temperature event has occurred. The DC-to-DC output bulk capacitance needs to be large enough to keep the FPGA and MRAM and/or DRAM running long enough to finish the next 4 steps. Most designs will easily meet the uptime requirement by meeting the bulk capacitance transient current requirements but should not be assumed. See the Board Level Checklist section below.
2. Finish all pending MRAM accesses at MIG top level. The control logic finishes delivering all data and status information to the MRAM MIG interface.

3. Set **power_fail_has_scramed** input signal to the MRAM MIG, and hold asserted. This tells the MIG that the control logic has finished and that the MIG should also scram, pushing all writes to the MRAM persistent array. It should also disable periodic reads. The control logic should not do reads and writes to the MRAM MIG while **power_fail_has_scramed** is asserted.
4. The **inflight_writes** signal is just a status output signal. After writes are done, the MIG executes a REFRESH command to close all open pages and store the data in the persistent memory array.
5. Wait for **cntr_power_fail_complete** output signal. This indicates that all pending writes in the MIG queue have been written into the MRAM persistent memory, and all pages are closed. Continue to hold MRAM MIG input signal **power_fail_has_scramed** asserted as it also disables periodic reads.
6. Once **cntr_power_fail_complete** is asserted out of the MIG, it is safe to power off MRAM without losing data.
7. If the control logic decides to start-up again (ex. after a power glitch) without an actual power-up reboot, the control logic can de-assert **power_fail_has_scramed** and the MIG will clear **cntr_power_fail_complete**. Periodic reads will be re-enabled, and normal reads and writes may begin again.

4.4 Performance

The following is a list of STT-MRAM optimizations to increase system performance.

1. Set address ordering/mapping for highest application performance and lowest wear to ROW-BANK-COL.
2. Increase command/data queue depths to enable look ahead activate/Precharge to manage the longer row access latencies and smaller CAS page sizes of STT-MRAM.
3. Achieving high bus utilization by accessing data on every clock edge.

5. DDR4 MIG Changes Using a Script

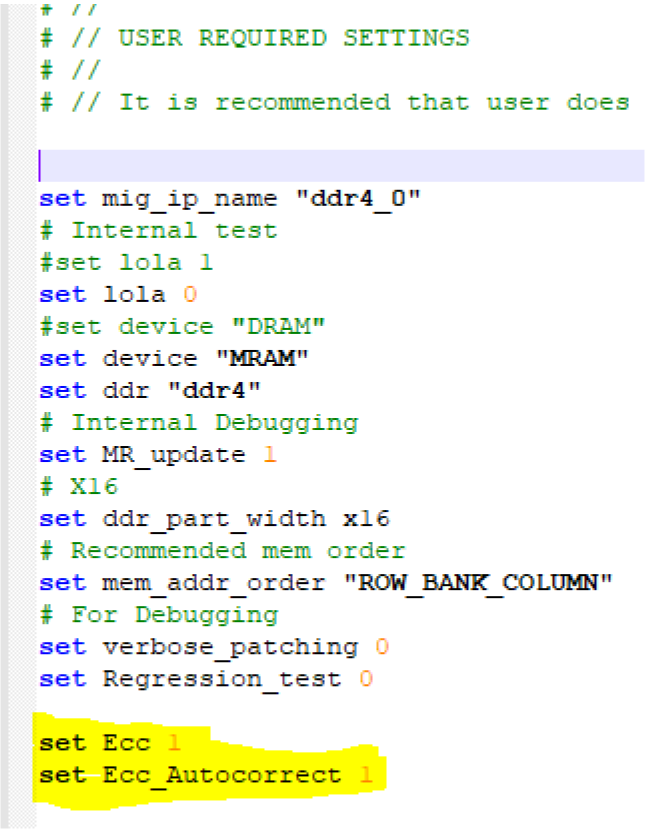
Everspin has made available an example script that will detect the user MIG version and apply the required RTL changes and updates to the MIG modules accordingly. Although this script is not externally supported, it is taken from the script Everspin uses internally. This script can be used by the engineer as a guide to manually make the require changes, or it may be modified as required to run in his/her own environment. You can locate this script on the Everspin website or from your Everspin representative.

5.1 Modified Design Flow

The design process for generating a MIG using the example script is similar to that of a standard Xilinx DDR4 MIG. Below is a suggested design process:

1. Create 8Gb DDR4 compatible MIG in Vivado
2. Create a simulation testbench by right clicking on the .xci file and selecting the Vivado menu item called "Open IP Example Design..." , Vivado creates a new project directory with the "_ex" appended to the end of the project name.
   The new project directory will look something like the following. **`/<home directory>/<user defined MIG name>_ex /<user defined MIG name>_0_ex.srcs/sources_1/ip/<user defined MIG name>/rtl`**
3. Simulate using the Xilinx generated testbench to ensure the 8Gb DDR4 MIG is operational.
4. The script has optional settings that can be set in the script itself. Most of the options are for debugging purposes, however if the user wants to use SEC/DED ECC within the MIG, he/she needs to make the following modification in the script:

   Change ***Set ECC 0*** to ***Set ECC 1***
   Change ***Set ECC_Autocorrect 0*** to ***Set ECC_Autocorrect 1***



```
# //
# // USER REQUIRED SETTINGS
# //
# // It is recommended that user does

set mig_ip_name "ddr4_0"
# Internal test
#set lola 1
set lola 0
#set device "DRAM"
set device "MRAM"
set ddr "ddr4"
# Internal Debugging
set MR_update 1
# X16
set ddr_part_width x16
# Recommended mem order
set mem_addr_order "ROW_BANK_COLUMN"
# For Debugging
set verbose_patching 0
set Regression_test 0

set Ecc 1
set Ecc_Autocorrect 1
```

Figure 1: Optional Setting in Script

We recommend that unless ECC is required in the MIG, the user uses the default settings.

5. Run the tcl script in Vivado Tcl console: src **patch_ddr4mig_mram_<*version*>.tcl**
6. The script parses the modules and reports all the modules that it patches successfully. If for any reason the script encounters an issue, it reports an error for the module being modified and for robustness it enables a self-checking mechanism to track against the expected patches. Be sure to check the final report at the completion of the script execution.
7. Re-Synthesize and Re-simulate your environment to ensure the updated 8Gb STT-DDR4 MIG is operational using the DDDR4 MRAM model (**st_mram_ddr4_model.sv**). This model is available from on the Everspin website or from your Everspin representative. There is a README file in the same location that should be the first step.

5.2 Modified MIG Modules

Table 3 below summarizes by category the modules that require changes from the standard Xilinx MIG controller for a XCKU060-2FFVA1156E device. When run properly, the example script will make these changes for you.

Table 3 - List of Modified Xilinx IP Modules.

Category	STT-MRAM Timing Parameter and Performance Changes	DDR4_0.sv	DDR4_0_DDR4.sv	DDR4_0_DDR4_mem_infc.sv	DDR4_v2_2_cal.sv	DDR4_v2_2_mc.sv	DDR4_v2_2_mc_arb_c.sv	DDR4_v2_2_mc_arb_mux_p.sv	DDR4_v2_2_mc_group.sv	Ddr4_v2_2_mc_ctl.sv	DDR4_v2_2_mc_ref.sv	DDR4_v2_2_ui.sv	Ddr4_v2_2_ui_cmd.sv	DDR4_v2_2_ui_rd_data.sv	DDR4_v2_2_ui_wr_data.sv	DDR4_v2_2_mc_periodic.sv
	File Number	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Timing	Timing settings and counter width changes		x			x		x	x							
Power-up	Anti-scribbling changes (NOMEM mode)				x											
Power-down	SCRAM input signal to drain writes with CAS page closes	x	x	x		x					x					
Power-down	Created SCRAM output status signals	x	x	x		x			x			x				
Performance	Auto pre-charges on the 8th BL8 of a CAS page		x			x				x		x	x	x	x	
Performance	FIFO-DEPTH doubled								x							
Performance	Changed to emit requests faster						x		x							x

5.1 DDR4 MIG Modified Output

The change table which will show the expected changes to the modules after running the script can be found on the Everspin website or from your Everspin representative. These changes are representative of those you should find in your modules. Your changes may differ slightly depending on parameters of your design. The file **ST-DDR4_Change_Table.docx** shows the changes after running the script with the default settings.

6. Collateral items

Please find the following collateral items on the Everspin website for download or by request.

1. ST-DDR4 TCL Script example file: **patch_ddr4mig_mram**<*version*>**.tcl**
2. Expected Changes to MIG modules document: **ST-DDR4_Change_Table.docx**
3. ST-DDR4 MRAM Verilog model: **st_mram_ddr4_model.sv** and **README.TXT**
4. Orcad schematic files for Everspin Test board (please contact Everspin)
5. Schematics in PDF format (please contact Everspin)
6. Allegro viewable board files (please contact Everspin)

7. Board Level Checklist

The following is a list of board level items the design engineer needs to consider to ensure a successful design.

1. Follow established high-speed routing and hardware design guidelines from the PCI-Sig, JEDEC, Xilinx and Micron for PCIe and DDR4 based designs.
2. The same high speed signaling layout guidelines and best practices that govern DDR4, also apply to ST-DDR4. Please see DDR4 SDRAM Unbuffered DIMM Design Specification (JEDEC login required). This same specification indicates the amount of bulk and decoupling capacitance required per device (See Table 9 of the DDR4 Unbuffered DIMM Design Specification).
3. Xilinx provides a PCB high speed design guideline that also includes the amount of decoupling and bulk capacitance required per device (see Table 1-12 in the UltraScale Architecture PCB User Guide). Xilinx also provides PCB high speed design guides for other families of devices too.
4. For STT-DDR4 power requirements (see Table 19 in the ST-DDR4 1Gb specification Everspin ST-DDR4 Specification).
5. For Xilinx FPGA power requirements, see the power estimator (XPE) Xilinx Power Estimator to estimate worst case power usage.

6. Schematic capture and FPGA pin assignments using the Xilinx Vivado development tool should be done iteratively to guarantee proper FPGA functionality and external signal routability.
7. As mentioned in the power-down section at the beginning of this document, a proper scramming sequence should take no longer than 10us. Meeting all bulk decoupling requirements for transient load changes will almost always be much more bulk capacitance needed to maintain a hold time beyond 10us. In most cases this will be in the 10's of ms range. This should not be assumed and should not replace calculating, simulating, and measuring the amount of hold time required for each design.
8. VDDQ, VDD, VrefCA, and VPP for ST-DDR4 are the same as the DDR4 1.2V specification (see Table 4 below).

Table 4 - Input voltages for ST-DDR4

Parameter	***JEDEC DDR4***	***1Gb ST-DDR4***
VDDQ, VDD	*1.2V, 1.2V*	*1.2V, 1.2V*
VPP	*2.5V*	*2.5V*
Vrefca	*VDDQ/2*	*VDDQ/2*

8. Conclusion

Everspin's STT-MRAM provides a superior alternative to DRAM-based controller architectures to solve I/O determinism problems, enable Enterprise Class performance and reliability without the need for alternate energy sources like batteries or supercapacitors to deliver byte addressable persistent memory. STT-MRAM allows designers to optimize footprint, performance, endurance, retention, and reliability at the same time reducing complexity and enabling advanced functionality.

Contact Information:

How to Reach Us:

www.everspin.com

E-Mail:

support@everspin.com
orders@everspin.com
sales@everspin.com

USA/Canada/South and Central America

Everspin Technologies
5670 W. Chandler Blvd, Suite 100
Chandler, AZ 85224
+1-877-347-MRAM (6726)
+1-480-347-1111

Europe, Middle East and Africa

support.europe@everspin.com

Japan

support.japan@everspin.com

Asia Pacific

Everspin Technologies, Inc.

Information in this document is provided solely to enable system and software implementers to use Everspin Technologies products. There are no express or implied licenses granted hereunder to design or fabricate any integrated circuit or circuits based on the information in this document. Everspin Technologies reserves the right to make changes without further notice to any products herein. Everspin makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Everspin Technologies assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. “Typical” parameters, which may be provided in Everspin Technologies data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters including “Typical” must be validated for each customer application by `-customer’s technical experts. Everspin Technologies does not convey any license under its patent rights nor the rights of others. Everspin Technologies products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Everspin Technologies product could create a situation where personal injury or death may occur. Should Buyer purchase or use Everspin Technologies products for any such unintended or unauthorized application, Buyer shall indemnify and hold Everspin Technologies and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Everspin Technologies was negligent regarding the design or manufacture of the part. Everspin™ and the Everspin logo are trademarks of Everspin Technologies, Inc. All other product or service names are the property of their respective owners.