

# Everspin MRAM DFN Package

## **8-Land DFN Packages**



8-land DFN Large Flag



8-land DFN Small Flag

- Compliant with RoHS, REACH regulations and practices.
- Contains no Red Phosphorus.
- Lead Free.
- All products meet MSL-3 moisture sensitivity level.
- Assembly with a JEDEC standard reflow profile.
- Can be placed on a standard SOIC footprint in most designs. See Application Note "Everspin's New 2mm Exposed Pad DFN Package Meets Both SOIC-8 and DFN8 PCB Layouts".

# Contents

Compliance with Environmental Regulations and Directives	2
Multiple Reflow Cycles and Moisture Resistance	2
Recommended Reflow Temperatures and Timing – All Packages	3
Thermal Resistance	4
Thermal Calculations	5
Package Outline Drawings	6
Revision History	11
Figure 1 - Recommended Reflow Profile _ All Packages	
Figure 2 - JEDEC PCB Thermal Model	
Figure 3 - Tj calculation using Ta	
Figure 4 - Package Outline 5x6 mm 8-Land DFN Large Flag (DESIGNATOR DC)	
Figure 5 - Package Outline 5x6 mm 8-Land DFN Small Flag (DESIGNATOR DF)	
Figure 6 - Package Outline 6x8 mm 8-Land DFN (DESIGNATOR DG)	
Figure 7 - Package Outline EMxxLXB 5x6 mm 8-Land DFN (DESIGNATOR DH)	10

1



## **Compliance with Environmental Regulations and Directives**

Environment	Statement Summary	Download Full Statement
RoHS	Everspin Technologies, Inc. MRAM products comply	Full RoHS Compliance
	with RoHS Directive 2002/95/EC.	<u>Statement</u>
REACH	Under the definition of the REACH regulations	Full REACH Statement
	EC1907/2006, Everspin Technologies is a producer	
	of "articles". REACH	
	requires article suppliers to inform recipients if an	
	article contains a Substance of Very High Concern	
	(SVHC) in excess of 0.1% by weight. Everspin	
	products do not contain any of these SVHC in excess	
	of 0.1% by weight.	
Red Phosphorus	Everspin Technologies, Inc. MRAM products do not	Full Red Phosphorus
	contain Red Phosphorus CAS# 7723-14-0 as an	<u>Statement</u>
	intentional additive.	
Environmental and	Materials from Conflict Regions Statement	Full Statement
Humanitarian		
Compliance		

## Multiple Reflow Cycles and Moisture Resistance

All Everspin packages are qualified by the procedure defined in IPC/JEDEC joint specification IPC/JEDEC J-STD-020D.1. They are guaranteed to withstand up to three reflow cycles without permanent damage, provided the conditions for the rated moisture resistance level for the part are observed prior to reflow.

Everspin parts are generally rated for MSL Level 3. Exceptions may exist and are noted in their respective data sheets. Please check the latest individual product data sheet to confirm the rated MSL for the product.

2



# Recommended Reflow Temperatures and Timing – All Packages

Everspin products can be assembled using a standard reflow profile. The profile below is based on IPC/ JEDEC J-STD-020D.1.

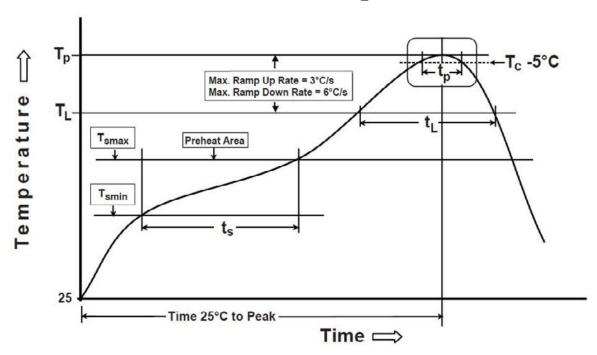


FIGURE 1 - RECOMMENDED REFLOW PROFILE ALL PACKAGES	FIGURE 1	- RECOMMENDED	<b>REFLOW PROFILE</b>	ALL PACKAGES
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Profile Step	Parameter	Symbol	Time/Temp	Unit
	Temperature minimum	T <sub>SMIN</sub>	150	°C
Preheat / Soak	Temperature maximum	T <sub>SMAX</sub>	200	°C
	Soak Time	ts	60 - 120	Seconds
	Rate from T <sub>L</sub> to T <sub>P</sub>	T <sub>L</sub> to T <sub>P</sub>	3° / Sec Max	° / Sec
Ramp Up	25°C to T <sub>p</sub>		8 minutes max	Minutes
	Liquidous Temperature	TL	217	°C
Reflow	Time Above T <sub>L</sub>		60 - 150	Seconds
	Peak Package Body Temperature	Τ <sub>Ρ</sub>	260	°C
	Time T <sub>c</sub> is within 5° of T <sub>P</sub>		30	Seconds
Ramp Down	Rate from T <sub>P</sub> to T <sub>L</sub>	T <sub>P</sub> to T <sub>L</sub>	6° / Sec Max	° / Sec

3

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## **Thermal Resistance**

Velocity (m/s)	Ambient Temp	Т <sub>J</sub> (°С)	Θ <sub>JA</sub> (°C/W)	
0	-40°C	-37.3	21.0	
0	85°C	87.7	31.9	

### TABLE 1 – THERMAL RESISTANCE 5x6 mm 8-LAND LARGE FLAG DFN (DESIGNATOR DC)

#### TABLE 2 - THERMAL RESISTANCE 5x6 mm 8-LAND SMALL FLAG DFN (DESIGNATOR DF)

Velocity (m/s)	Ambient Temp	Т <sub>ј</sub> (°С)	Θ <sub>JA</sub> (°C/W)	Θ <sub>JB</sub> (°C/W) 1	⊖ <sub>JC</sub> (°C/W)	Ψ <sub>JB</sub> (°C/W)	Ψ <sub>JT</sub> (°C/W) 2
0		34.7	57.7			30.2	0.38
1	25%0	33.1	48.0	32.5	1.8	29.0	0.88
2	25°C	32.7	45.9			28.5	1.10
3		32.5	44.6			28.1	1.26

#### Notes:

- 1.  $\Theta_{JB}$  value assumes 4-layer PCB.
- 2.  $\Psi$  is a thermal characterization factor indicating the temperature rise between package top and the device junction. See JESD51-2.

#### TABLE 3 - THERMAL RESISTANCE EMXXLX 6x8 mm 8-LAND DFN (DESIGNATOR DH)

Die Stack	Ta (C)	Package Size (mm)	Θ <sub>JA</sub> (0	C/W)	Θ <sub>JB</sub> (C/W)	Θ <sub>JC</sub> (C/W)	Ψ <sub>」</sub> (c/\	
			0 m/s	1 m/s			0 m/s	1 m/s
x1	25	8x6	36.9	23.5	18.8	5.7	0.1	0.68
x2	25	8x6	36.8	28.4	20.0	6.8	0.25	0.63

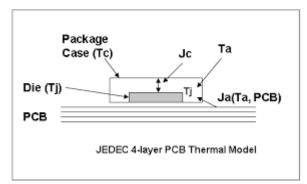
Velocity (m/s)	Ambient Temp	Т <sub>Ј</sub> (°С)	Θ <sub>JA</sub> (°C/W)	Θ <sub>JB</sub> (°C/W)	Θ <sub>JC</sub> (°C/W)	Ψ <sub>JB</sub> (°C/W)	Ψ <sub>JC</sub> (°C/W)
0		48.1	46.0			20.3	1.2
1	25%	43.9	37.9	20.4	177	20.0	1.7
2	25°C	43.1	36.2	20.4	17.7	19.8	2.0

#### TABLE 4 THERMAL RESISTANCE EMXXLXB 5x6 mm 8-LAND DFN (DESIGNATOR DH)

## **Thermal Calculations**

Designers may require different thermal numbers for specific models or environments. Figure 2 below depicts the JEDEC thermal resistances of typical packages. Using the thermal resistances and power provided in the device specific data sheet, and using industry standard equations, the desired thermal variable can be calculated. Figure 3 depicts an example calculation using Ta to calculate Tj.

#### FIGURE 2 - JEDEC PCB THERMAL MODEL





Tj = Ta + Rth(j-a)×P
Ta : Temperature of ambient atmosphere (= room temperature where the measurement was done)
Rth(j-a) : Thermal resistance inbetween Junction and Ambient atmosphere *
P : Power dissipation **

5

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## Package Outline Drawings

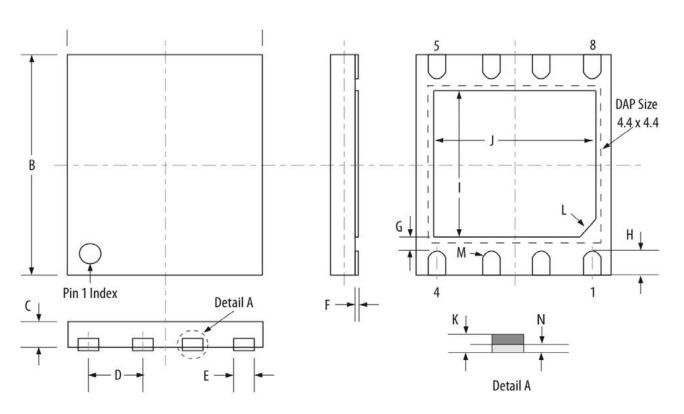


FIGURE 4 - PACKAGE OUTLINE 5x6 mm 8-LAND DFN LARGE FLAG (DESIGNATOR DC)

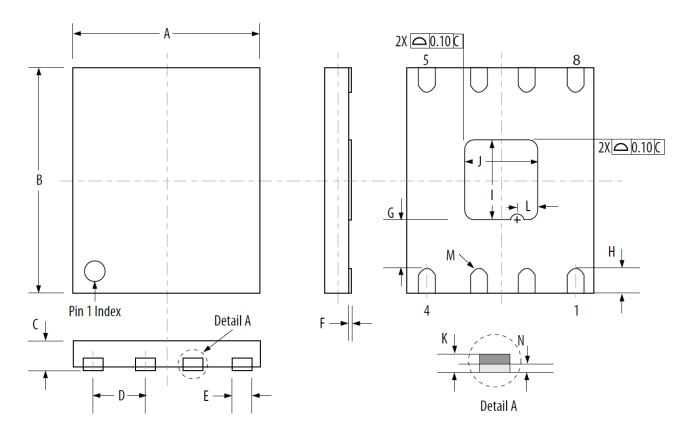
Dimension	Α	В	С	D	E	F	G	Н	I	J	К	L	М	Ν
Max.	5.10	6.10	1.00	1.27	0.45	0.05	0.35	0.70	4.20	4.20	0.261	C0.35	R0.20	0.05
Min.	4.90	5.90	0.90	BSC	0.35	0.00	Ref.	0.50	4.00	4.00	0.195	0.55	1.0.20	0.00

Notes:

1. All dimensions are in mm. Angles in degrees.



- 2. Coplanarity applies to the exposed pad as well as the terminals. Coplanarity shall be within 0.08 mm.
- 3. Warpage shall not exceed 0.10 mm.
- 4. Refer to JEDEC MO-229
- 5. Lead plating 400 800  $\mu m$  Sn.



#### FIGURE 5 - PACKAGE OUTLINE 5x6 mm 8-LAND DFN SMALL FLAG (DESIGNATOR DF)

Dimension	Α	В	C	D	E	F	G	н	I	J	К	L	М	Ν
Max	5.10	6.10	0.90	1.27	0.45	0.05	1.60	0.70	2.10	2.10	.210	C0.45	R0.20	0.05
Min	4.90	5.90	0.80	BSC	0.35	0.00	1.20	0.50	1.90	1.90	.196	C0.45	KU.2U	0.00

7

NOTE:

1. All dimensions are in mm. Angles in degrees.



- 2. Coplanarity applies to the exposed pad as well as the terminals. Coplanarity shall be within 0.08 mm.
- 3. Warpage shall not exceed 0.10 mm.
- 4. Refer to JEDEC MO-229
- 5. Lead plating 300 600  $\mu$ m Sn.

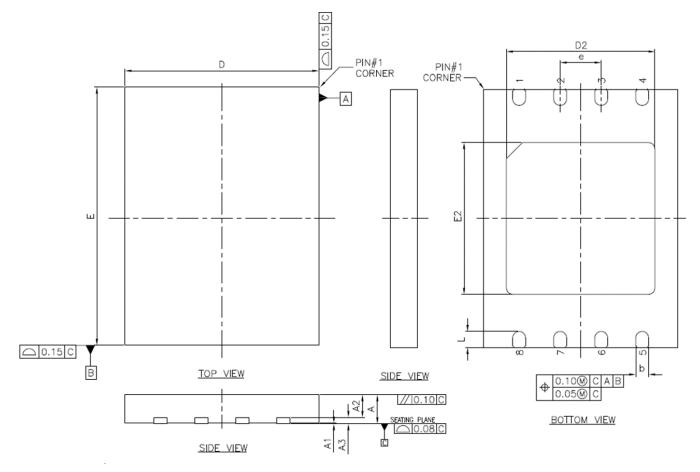


FIGURE 6 - PACKAGE OUTLINE 6x8 MM 8-LAND DFN (DESIGNATOR DG)



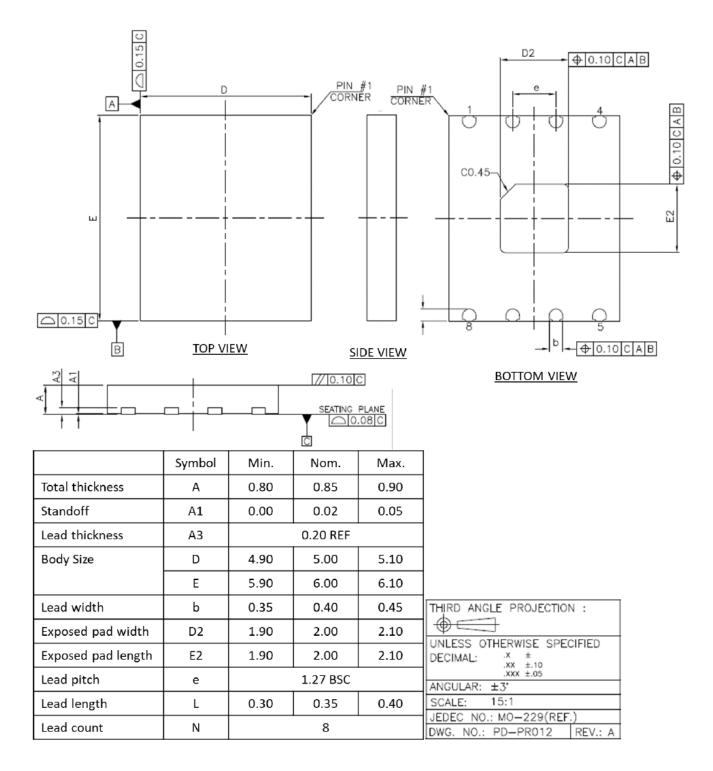
# Everspin MRAM DFN Package

	Symbol	Min.	Nom.	Max.				
Total thickness	А	0.85	0.90	0.95				
Standoff	A1	0.00	0.02	0.05				
Mold thickness	A2	0.65	0.70	0.75				
Lead thickness	A3		0.20 REF		THIRD ANGLE PROJECTION			
Body Size	D	5.90	6.00	6.10				
	E	7.90	8.00	8.10	UNLESS OTHERWISE SPECIFIED			
Lead width	b	0.35	0.40	0.48	DECIMAL: .X <u>+</u>			
Exposed pad width	D2	4.55	4.60	4.65	.XX <u>+</u> .10 .XXX <u>+</u> .05			
Exposed pad length	E2	4.65	4.70	4.75	ANGULAR + 3°			
Lead pitch	E		1.27 BSC		SCALE: 15:1			
Lead length	L	0.45	0.50	0.55	JEDEC NO.: MO-229(REF.)			
Lead count	Ν		8L		DWG. NO.: PD-PR23 (OSE) REV.: A			

9









# **Revision History**

Revision	Date	Description of Change
1.0	October 24,2013	Initial Release
1.1	October 21, 2014	Added Reflow Cycle and Moisture Resistance section.
1.2	April 12, 2018	Updated the Contact Us table
1.3	June 28, 2022	Added 6x8 mm 8 – Land DFN package information
1.4	February 7, 2023	Added Thermal Calculation section. Updated formatting to conform with latest Everspin format template.
1.5	August 18, 2023	Added Table 4: Thermal Resistances EMxxLXB 5x6 mm DFN 8-Land Added Figure 7: Package Outline EMxxLXB 5x6 mm DFN 8-Land Compliance document links updated



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