

Introduction

This user guide is provided to help users understand the Hardware and Software requirements needed for evaluation of the EMxxLX Industrial STT MRAM device from Everspin.

This guide will outline the Hardware and Software requirements for the user to setup, configure, initialize, and generate traffic test vectors for the EMxxLX device.

This guide assumes the user has full access to the EMxxLX data sheet and a reasonable understanding of HW and SW usage. This guide makes references and links to other support documents for the user.

Contents

Intr	Introduction1			
List	List of Figures and Tables			
1.	EMxxLX Daughter Card	2		
2.	Required Host Board Support	3		
3.	IDE (Integrated Development Environment) Support	4		
4.	Memory Controller Support	5		
5.	IDE Software Installation and Configuration	5		
6.	Hardware connection, FPGA Image and .ELF file download	5		
7.	Reading and Writing EMxxLX MRAM	5		
Summary				
Rev	Revision History			



List of Figures and Tables

Figure 1	EMxxLX Daughter Card	.2
Figure 2	CRUVI CR00100-01	.4

1. EMxxLX Daughter Card

The EMxxLX Daughter Card is populated with Everspin EMxxLX 64Mbit Industrial STT MRAM device. Other EMxxLX densities can be populated as well. This device is obtained through the sample request form on Everspin's website located here:

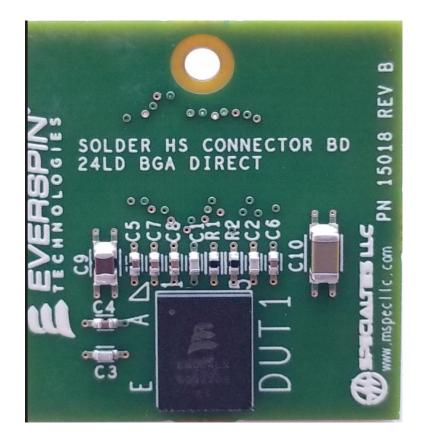


FIGURE 1 EMXXLX DAUGHTER CARD



2. Required Host Board Support

The EMxxLX evaluation board, here in referenced as the EMxxLX daughter card is designed to connect to the Open FPGA specification CRUVI CR00100-01 host board HS (High Speed) slot. This host platform is available to order from Trenz Electronic LLC website: <u>https://shop.trenz-electronic.de/en/CR00100-01-DBC82A-CRUVI-MAX-10-Base-Board-with-Intel-MAX-10-FPGA-8-MByte-SDRAM-4.5-x-5.7-cm?c=579</u>

The CR00100-01 board has the following key features:

- On Board
 - o JTAG and UART over Micro USB connector
 - 2 x User Push button
 - 4 x User LEDs (red, green)
- SoC/FPGA
 - Intel MAX10 FPGA (10M08 as standard option)
- RAM/Storage
 - 8 MByte SDRAM
- Interface
 - o 1 x CRUVI LS
 - o 1 x CRUVI HS
- Power
 - Power from micro USB connector
- Dimension
 - o 44.86 mm x 57.50 mm





FIGURE 2 CRUVI CR00100-01

3. IDE (Integrated Development Environment) Support

The Intel Max10 FPGA is supported using the Intel [®] Quartus Prime Lite Edition Design Software. The LITE edition is a free use IDE and is available for download from Intel [®] web site located here: <u>https://www.intel.com/content/www/us/en/software-kit/684216/intel-quartus-prime-lite-edition-design-software-version-21-1-for-windows.html</u>

Along with the IDE it is highly encouraged users download the Intel ® recommended documentation.

Documentation Links:

- Intel® Quartus® Prime Software User Guides
- Intel® FPGA Software Installation and Licensing Manual
- Intel® Quartus® Prime Software and Device Support Release Notes (PDF)



4. Memory Controller Support

EMxxLX is Everspin's latest Industrial STT MRAM supporting JESD251 Expanded Serial Peripheral Interface (xSPI). To properly support this new JEDEC standard an xSPI compatible memory controller is required. Synaptic Labs LLC MBMC (Multi-Bus Memory Controller) IP is used in this evaluation board.

The Memory Controller IP temporary license (.lic) file is provided by Synaptic Labs LLC. Link for requesting temporary license file is here: <u>https://synaptic-labs.com/free-trial-request/</u>

After contacting and receiving the temporary license file, follow all directions contained in the Synaptic guide for installing and configuring the Memory controller IP.

5. IDE Software Installation and Configuration

To program the FPGA with the correct image Quartus Prime IDE is used in conjunction with Synaptic Labs MBMC (Multi-Bus Memory Controller) IP. Locate the Quartus Prime IDE install file downloaded in section 3. Follow the installation instructions associated with the file. The user guide assumes default file location is used during the installation process.

6. Hardware connection, FPGA Image and .ELF file download

To program the Max10 FPGA a Micro-USB cable with data connection is required. Ensure the cable supports data transfer and not just charging capabilities.

A USB Programmer is required for image download to the FPGA. The arrow USB programmer is used for this task.

The SW and installation instructions are located here:

https://wiki.trenz-electronic.de/display/PD/Arrow+USB+Programmer

After installation of the Arrow USB programmer the CR00100-01 board is ready for the FPGA image download.

7. Reading and Writing EMxxLX MRAM

Contained within the Synaptic user guide are instructions for reading and writing the EMxxLX device.

Summary

This Evaluation platform user guide has been provided to give users the ability to evaluate Everspin's EMxxLX Industrial MRAM.

The detailed steps provide users the required download and installation instructions for the Integrated Development Environment (IDE), SW support packages, License files and USB programming tools. After proper configuration, the user can download the required FPGA .SOF and ELF files to test and evaluate EMxxLX industrial MRAM.



Revision History

Revision	Date	Description of change
1.0	October 12, 2022	Initial Release
1.1	March 15, 2023	Updated license file installation instructions
1.2	September 28, 2023	Updated User Guide naming convention to identify Intel
		FPGA based host board.
1.3	November 10, 2023	Updated Memory Controller support section



Contact Information:

Author: Daniel Symalla

Senior FAE

WW Sales Group

How to Reach Us:

www.everspin.com

E-Mail:

support@everspin.com

orders@everspin.com

sales@everspin.com

USA/Canada/South and Central America

Everspin Technologies

5670 W. Chandler Road, Suite 100

Chandler, Arizona 85226

+1-877-347-MRAM (6726)

+1-480-347-1111

Europe, Middle East and Africa

support.europe@everspin.com

Japan

support.japan@everspin.com

Asia Pacific

support.asia@everspin.com

Everspin Technologies, Inc.

Information in this document is provided solely to enable system and software implementers to use Everspin Technologies products. There are no express or implied licenses granted hereunder to design or fabricate any integrated circuit or circuits based on the information in this document. Everspin Technologies reserves the right to make changes without further notice to any products herein. Everspin makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Everspin Technologies assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters, which may be provided in Everspin Technologies data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters including "Typical" must be validated for each customer application by customer's technical experts. Everspin Technologies does not convey any license under its patent rights nor the rights of others. Everspin Technologies products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Everspin Technologies product could create a situation where personal injury or death may occur. Should Buyer purchase or use Everspin Technologies products for any such unintended or unauthorized application, Buyer shall indemnify and hold Everspin Technologies and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Everspin Technologies was negligent regarding the design or manufacture of the part. Everspin™ and the Everspin logo are trademarks of Everspin Technologies, Inc. All other product or service names are the property of their respective owners.