Everspin Expands Spin-transfer Torque MRAM Ecosystem Support for its 1 Gigabit STT-MRAM with Cadence Design IP and Verification IP

(Flash Memory Summit) SANTA CLARA, Calif. – August 05, 2019 — Everspin Technologies, Inc., (NASDAQ: MRAM), the world's leading developer and manufacturer of Magnetoresistive RAM (MRAM), announced it is expanding the ecosystem for its 1 Gb Spin-transfer Torque MRAM (STT-MRAM) with Cadence Design Systems, Inc. providing DDR4 Design IP (DIP) and Verification IP (VIP) support for Everspin's 1 Gb STT-MRAM memory.

Cadence and Everspin have collaborated together on multiple projects, and Cadence has supported Everspin's STT-MRAM products since 2012. With Cadence® controller IP and VIP solutions, Everspin customers will be able to request MRAM-enabled IP and VIP for their Custom ASIC solutions. Everspin's 1 Gb STT-MRAM product family includes both 8-bit and 16-bit DDR4 compatible (ST-DDR4) interface versions of the device and are available in a JEDEC-compliant BGA package.

"Our customers are inquiring about DIP and VIP support, so they can create new ASIC solutions which will support Everspin STT-MRAM," said Everspin's Vice President of Marketing Rizwan Ahmed. "Everspin's growing ecosystem is now supported by Cadence controller IP and VIP solutions, which are used broadly in storage systems."

Everspin's STT-MRAM 1 Gb part offers more effective management of I/O streams, creating a greater level of latency determinism and allowing storage OEMs to significantly improve quality of service of their products. Customers requiring DIP and VIP support to enable Everspin's 1 Gb STT-MRAM can now work with Cadence to achieve it.

"The compatibility of Cadence DIP and VIP with Everspin's STT-MRAM will provide systems developers the ability to implement a high-speed, persistent memory host controller and PHY in advanced SoCs," said David Peña, product management director, VIP at Cadence. "We are pleased to be working with Everspin to bring advanced persistent memory capability to modern data center storage and computing applications."

The Cadence IP portfolio supports the company's Intelligent System Design strategy, which enables system and semiconductor companies to create complete, differentiated end products more efficiently. Customers benefit from having access to a complete, single-vendor solution for controller, PHY and VIP that speeds chip integration time and reduces interoperability risk.

About Everspin Technologies

Headquartered in Chandler, Arizona, Everspin Technologies, Inc. is the worldwide leader in the design, volume production and distribution of Magnetoresistive RAM (MRAM) into markets and applications where data persistence, performance, and endurance are paramount. Serving applications across the data center, industrial, and transportation markets, Everspin has built the strongest and fastest-growing foundation of MRAM users in the world. For more information, visit **www.everspin.com**.

Cautionary Statement Regarding Forward-Looking Statements

This press release contains forward-looking statements regarding future events that involve risks and uncertainties that could cause actual results or events to differ materially from the expectations disclosed in the forward-looking statement, including, but not limited to; the anticipated market adoption of Everspin's products and technology at the rate Everspin expects; the ability for Everspin to expand the markets Everspin addresses at the rate it expects; the risk that unexpected technical difficulties may develop in the final stages of development or production of its products, or when Everspin's customers may ship in volume. Readers are advised that they should not place undue reliance on these forward-looking statements and should review the risk factors included in Everspin's Form 10-Q filed with the Securities and Exchange Commission on May 9, 2019, under the caption "Risk Factors." Subsequent events may cause these expectations to change, and Everspin disclaims any obligations to update or alter these forward-looking statements in the future, whether as a result of new information, future events or otherwise.

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