

Replacing the Cypress CY62137FV18LL MoBL SRAM with Everspin's MR1A16AxMA35 MRAM

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EVERSPIN MRAM MEMORY

Everspin is the worldwide leader in designing, manufacturing, and commercially shipping discrete Magnetoresistive RAM (MRAM) into markets and applications where data persistence and integrity, low latency, and security are paramount.

RELIABLE SUPPLY

Everspin is a long term, reliable manufacturer of MRAM products and operates a fabrication facility in Chandler, Arizona.

OVERVIEW

The Everspin 2Mb MRAM M1A16AxMA35 can operate with the Cypress 2Mb SRAM CY62137FV18LL slower timing, but also allows the system designer to take advantage of MRAM's faster random access cycle time. The Everspin 2Mb MRAM M1A16Axxx35 is available in 48-BGA.

BENEFITS OF MR1A16AxMA35

Upgrading to Everspin MRAM provides many benefits over Cypress SRAM:

- Faster Random Access Operation Times
- High Reliability and Data Retention
- Unlimited Read/Write Endurance
- No Wear-out Concern
- Competitive Pricing
- Stable Manufacturing Supply Chain
- Standard BGA package

GENERAL CONSIDERATIONS FOR REPLACING SRAM WITH MRAM

Everspin Toggle technology magnetic RAM (MRAM) is essentially non-volatile SRAM. Replacing SRAM with MRAM in any application adds non-volatility without compromise of performance or function. Replacing a volatile SRAM with MRAM will provide instant 20-year data retention without the overhead of storing data to a non-volatile cell or the expense and space of a battery backup power source.

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CONSIDERATIONS FOR REPLACING CYPRESS CY62137FV18LL (128k x 16) MoBL SRAM with EVERSPIN MR1A16AxMA35 (128k x 16) MRAM

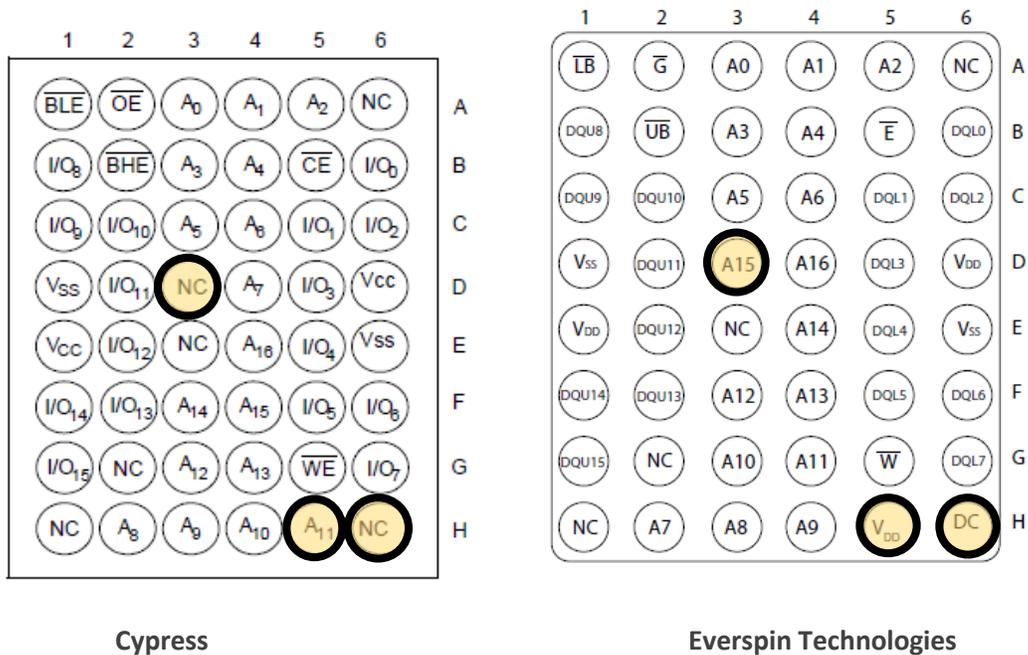
Designers considering a replacement of CY62137FV18LL with MR1A16AxMA35 need to consider differences in package size and timing. Everspin MR1A16AxMA35 has a different operating voltage range from 3.0V to 3.6V, with a typical of 3.3V.

Table 1 – Overview: CY62137FV18LL-45BVx vs. MR1A16AxMA35

Parameter	CY62137FV18LL	MR1A16AxMA35
Package	48 Ball VFBGA	48 Ball BGA
Size and Height	6 × 8 × 1.0 mm	10 x 10 x 1.35 mm
Pinout / Footprint	See Figure 2 and Table 4 below	
Solder Profile	Per JEDEC J-STD-020D.1	
Firmware / Timing	Ons Address Hold Time	12ns Minimum Address Hold Time. See Figure 7 below

Figure 1 – Pinout/Footprint Comparison and Considerations

48 BALL BGA



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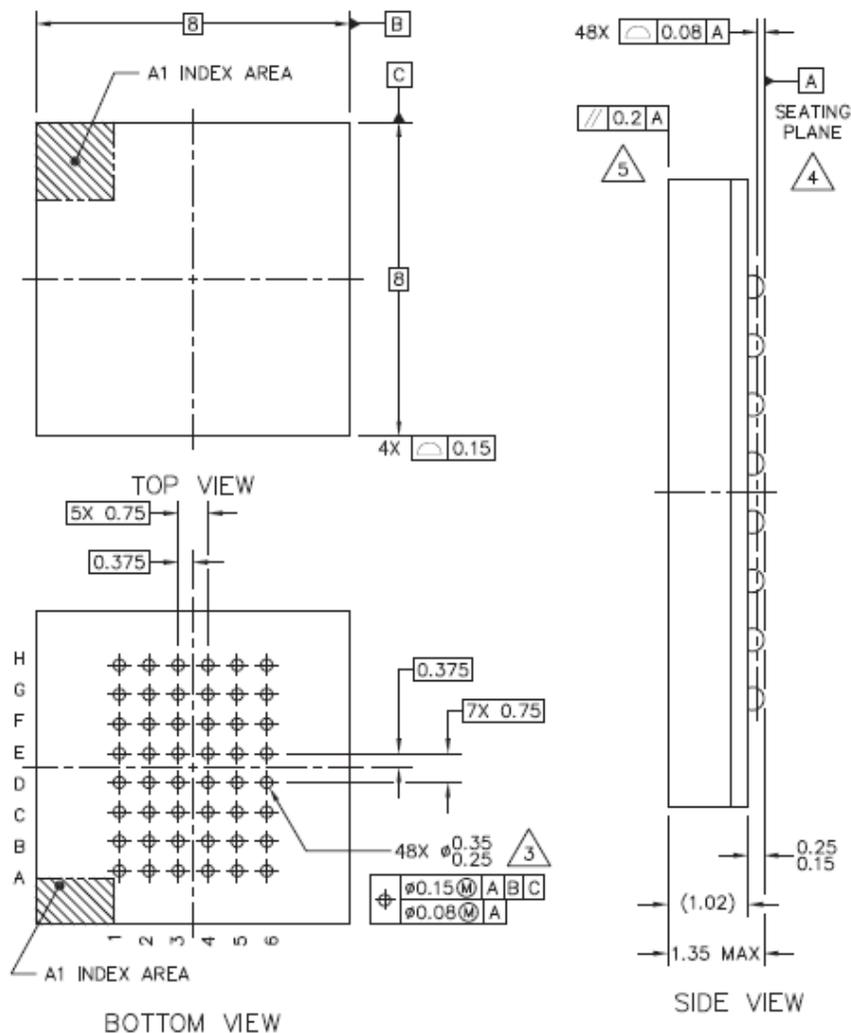
Table 2 – Pin Function Comparison

Ball #	Cypress	Everspin	Everspin Definition	Everspin Comments
D3	NC	A15	Address Input	
H5	A11	Vdd	Power Supply	
H6	NC	DC	Do Not Connect	This pin is used for test. Prefer to float. If driven, must be pulled to VIL.

PACKAGE COMPATIBILITY

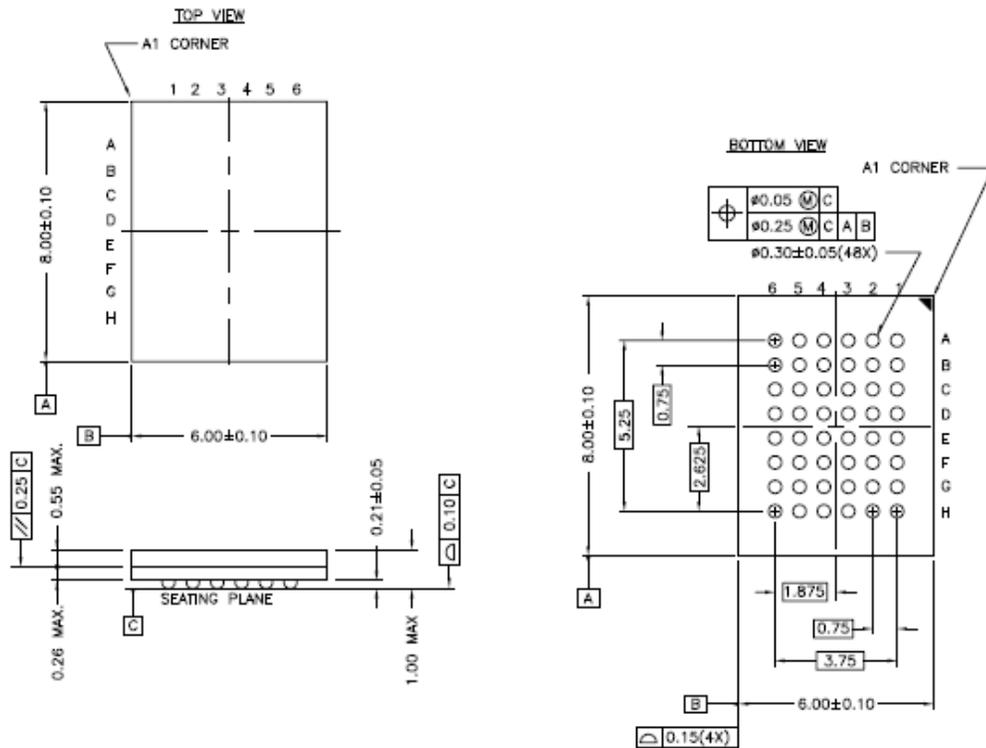
The Everspin Technologies 48 Ball BGA package is a close-fit with the corresponding Cypress equivalent. However, see figure 4 and 6 to understand the package dimension differences between the Cypress and Everspin FBGA packages. Make special note of the package dimension differences requiring different mechanical “Keep out” areas for these packages. Please refer to the current datasheet for details.

Figure 2 – EVERSPIN Package Outline 10x10mm 48-BGA



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Figure 3 – Cypress Package Outline 6 x 8 x 1mm 48-VFBGA

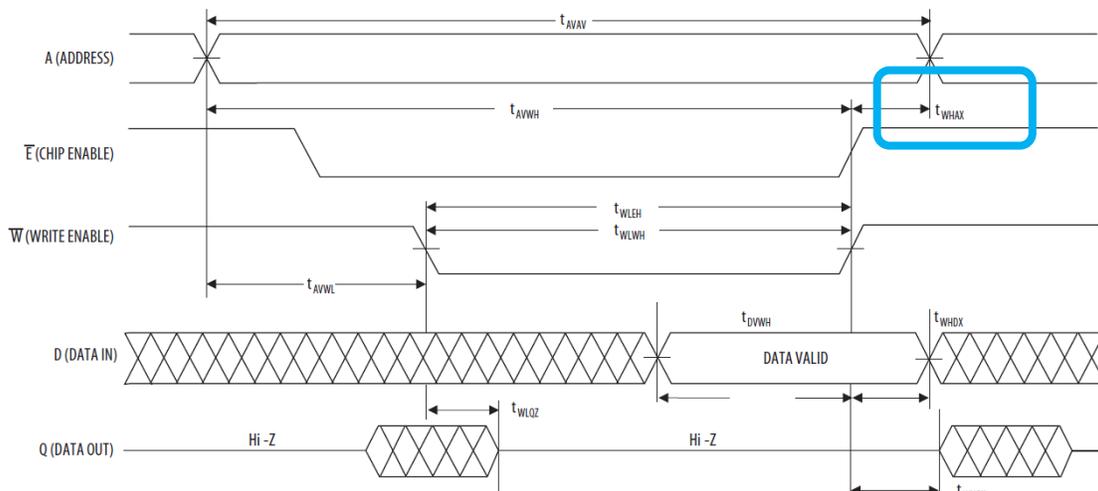


OTHER REPLACEMENT DESIGN CONSIDERATIONS

MRAM ADDRESS HOLD TIME

The Address Hold Time (Everspin Write Recovery Time, t_{WHAX}) for the M1A16AxMA35 is a minimum of 12ns compared to 0ns minimum for CY62137FV18LL.

Figure 7 – 12ns Minimum for Address Hold Time for MR1A16Axxx35



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Due to its persistence, there is no power monitoring requirement for the Everspin MRAM as is the case with the SRAM. Hence initiating or monitoring Hardware Stores, Re-stores and associated software routines are unnecessary and can be eliminated.

SIMPLIFIED POWER CYCLING

When power is removed from the MRAM, data remains valid over 20 years' time and across the temperature range. This feature, unique to MRAM, allows for Duty Cycle Power control enabling the user to reduce their overall power consumption without concern of wear-out or lost data.

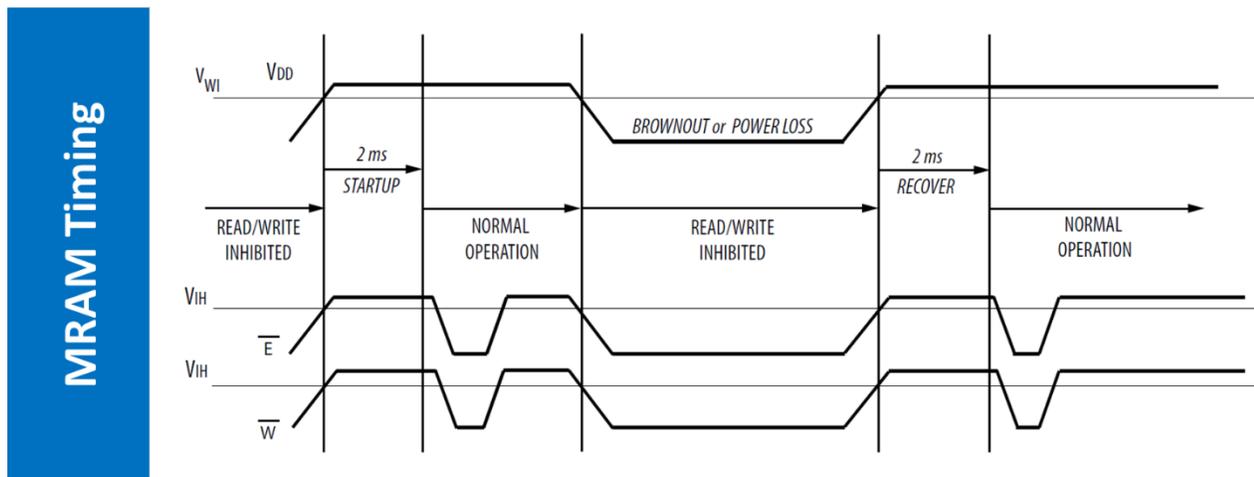
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The MRAM is protected from write operations whenever VDD is less than VWI. As soon as VDD exceeds VDD(min), there is a startup time of 2 ms before read or write operations can start. This time allows memory power supplies to stabilize.

The \overline{E} and \overline{W} control signals should track VDD on power up to $VDD - 0.2\text{ V}$ or V_{IH} (whichever is lower) and remain high for the startup time. In most systems, this means that these signals should be pulled up with a resistor so that a signal remains high if the driving signal is Hi-Z during power up. Any logic that drives \overline{E} and \overline{W} should hold the signals high with a power-on reset signal for longer than the startup time. During power loss or brownout where VDD goes below VWI, writes are protected, and a startup time must be observed when power returns above VDD(min).

MRAM POWER-UP SEQUENCING

Both MRAM and SRAM will operate from different power supply ranges. Both MRAM and SRAM have similar active operating currents, however, the "Start-up" time for the MRAM is 2ms vs. 55ns for the SRAM. Proper decoupling capacitors should be used to assure reliable operation. The power loss/startup sequence for the MRAM is shown below:



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SUMMARY

Replacing a CY62137FV18LL with Everspin's M1A16AxMA35 2Mb MRAM is a straight-forward process. These devices are close to a drop-in replacement with some consideration of pinout, timing and power supply details shown in the application note.

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